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Channel Mapping on the PreProcessor Module (PPM)

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This mini-document describes channel mapping through the PPM from the analogue input connectors to the digital LVDS output connectors. The aim has been to collect, and correlate, all existing naming conventions from different documentations. What this note does not provide is a correlation between channel number on the PreProcessor System and the (ϕ,η) coordinates of the calorimeter Trigger Towers. The Cable Mapping documentation[1] should be consulted for cross reference.

Analogue channel numbering on the front panel of the PPM and the corresponding channel configuration within the analogue connectors are depicted in the diagram on Figure 2. The diagram displays PPM's front panel, viewed from the front of the crate. To be noted is the top-down numbering scheme of the analogue channels along the front panel of the PPM. Notice on the other hand the bottom-up numbering scheme on the pin-pairs within the analogue connectors.

The digital LVDS compactPCI connector on the backplane of the PPM, viewed from the back of the crate, is shown on Figure 3. Several things should be noted here. The connector is vertically partitioned in two sections, the upper one to transmit Cluster Processor signals and the lower one to transmit Jet/Energy Processor signlas. A top-down numbering scheme is adopted for pin positions, as indicated to the left of the connector on the figure. The layout of the LVDS backplane connector is such that the unused pin positions are at the center, effectively separating Links to CPM from links to JEM. Naming convention adopted in [1] is indicated to the right of the connector on Figure 3. The partitioning within each section reflects the modularity of the LVDS cable connectors, carrying four differential pairs each. The polarity and labeling of the pin pairs inside an LVDS cable connector is also depicted on the diagram in this figure.

Figure 1: Cable connector carrying four LVDS links. Viewed from the front (looking into the connector).

Channel mapping across the PPM, with reference to the analogue and digital channel numbering conventions, along with pin allocations within the LVDS connectors, are shown on Tables 1 and 2 for CPM Links and on Tables 3 and 4 for JEM Links. Color codes on these tables should guide the eye to track channels across PPM, i.e. to be able to correlate more easily analogue and digital channels on board.

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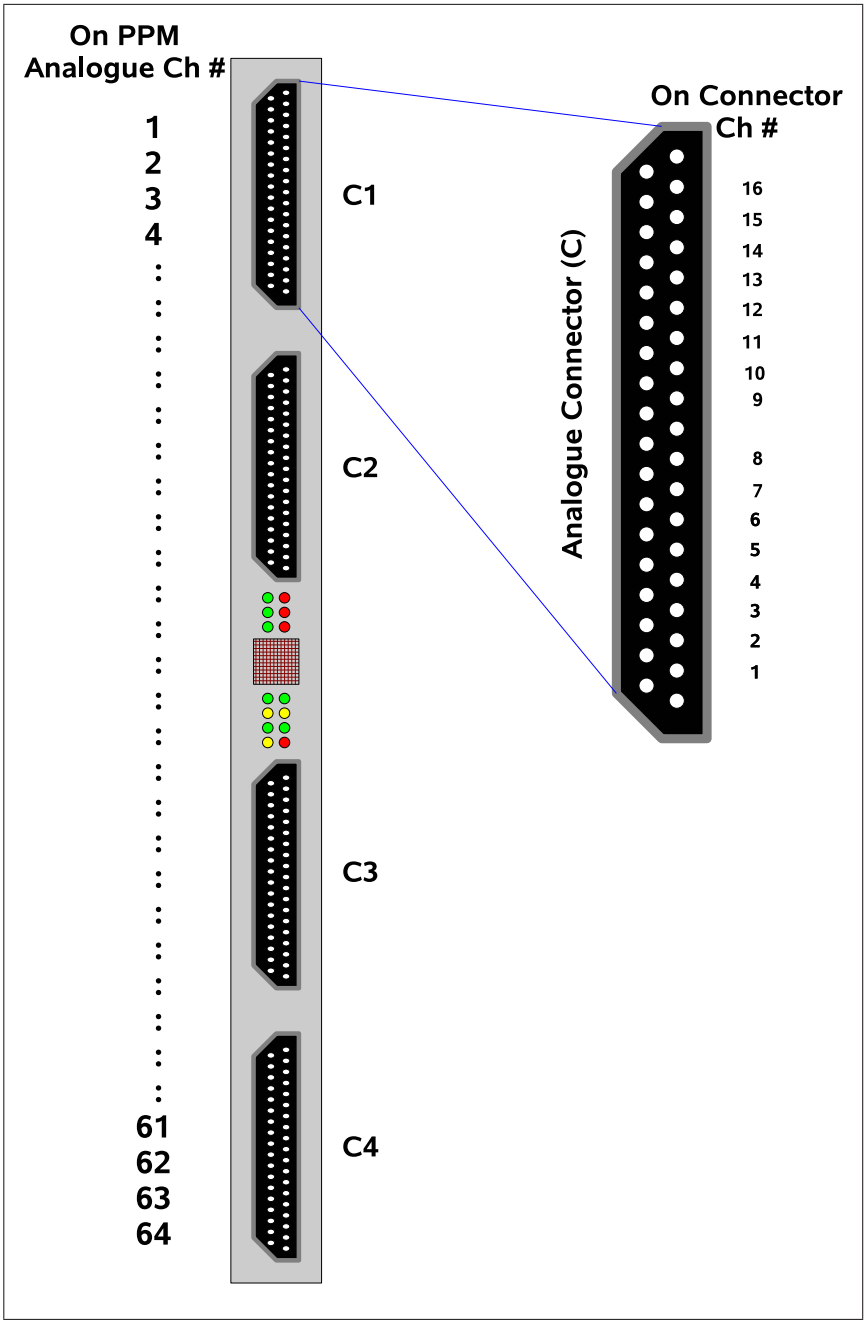

Figure 2: Analogue channel numbering scheme on the PPM front panel. A total of 64 trigger tower signals are received on 4 analogue (input) connectors, each carrying 16 channels. To be noted is the top-down (bottom-up) numbering scheme on the front panel (connector).

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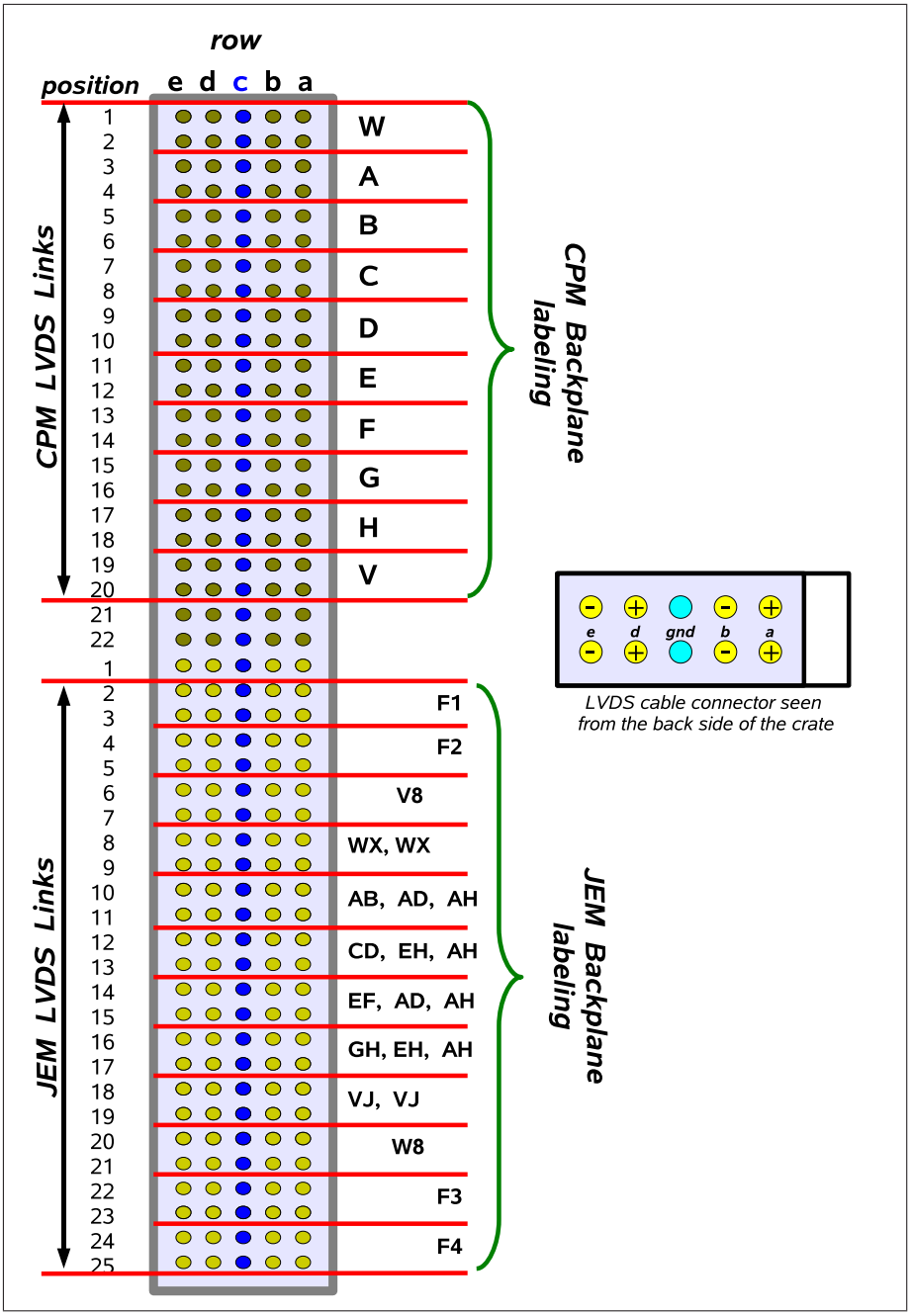

Figure 3: PPM compactPCI backplane connector for LVDS links, as seen from the back of the crate. Please note the pin position numbering on the left. Ranges for CPM and JEM LVDS links with reference to the nomenclature in [1] is indicated to the right of the connector. Also displayed is an LVDS cable connector, looking through the connector from the back. Polarity and labeling of the pins are also indicated.

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Table 1: PPM channel mapping for CPM LVDS links, for channels 1 to 32, corresponding to the upper two analogue connectors on the front panel. C: Connector; FP: Front Panel; BP: Back Plane.

Analog C ch#	Analog FP ch#	MCM slot #	MCM ch map	Digital ch#	PPM to CPM LVDS Connector	PPM/CPM BP
					mcm # 1: D3 & D4, D1 & D2 mcm # 2: D7 & D8, D5 & D6	W/w
C1_A16	A1	1	A1	D1	mcm # 1: D3 & D4, D1 & D2 mcm # 2: D7 & D8, D5 & D6	A/a
C1_A15	A2		A4	D2		
C1_A14	A3		A2	D3		
C1_A13	A4		A3	D4		
C1_A12	A5	2	A5	D5		
C1_A11	A6		A8	D6		
C1_A10	A7		A6	D7		
C1_A9	A8		A7	D8		
C1_A8	A9	3	A9	D9	mcm # 4: D15 & D16, D13 & D14 mcm # 3: D11 & D12, D9 & D10	B/b
C1_A7	A10		A12	D10		
C1_A6	A11		A10	D11		
C1_A5	A12		A11	D12		
C1_A4	A13	4	A13	D13		
C1_A3	A14		A16	D14		
C1_A2	A15		A14	D15		
C1_A1	A16		A15	D16		
C2_A16	A17	5	A17	D17	mcm # 5: D19 & D20, D17 & D18 mcm # 6: D23 & D24, D21 & D22	C/c
C2_A15	A18		A20	D18		
C2_A14	A19		A18	D19		
C2_A13	A20		A19	D20		
C2_A12	A21	6	A21	D21		
C2_A11	A22		A24	D22		
C2_A10	A23		A22	D23		
C2_A9	A24		A23	D24		
C2_A8	A25	7	A25	D25	mcm # 8: D31 & D32, D29 & D30 mcm # 7: D27 & D28, D25 & D26	D/d
C2_A7	A26		A28	D26		
C2_A6	A27		A26	D27		
C2_A5	A28		A27	D28		
C2_A4	A29	8	A29	D29		
C2_A3	A30		A32	D30		
C2_A2	A31		A30	D31		
C2_A1	A32		A31	D32		

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Table 2: PPM channel mapping for CPM LVDS links, for channels 33 to 64, corresponding to the lower two analogue connectors on the front panel. C: Connector; FP: Front Panel; BP: Back Plane.

Analog C ch#	Analog FP ch#	MCM slot #	MCM ch map	Digital ch#	PPM to CPM LVDS Connector	PPM/CPM BP
C3_A16	A33	9	A33	D33	mcm # 9: D35 & D36, D33 & D34 mcm # 10: D39 & D40, D37 & D38	E/e
C3_A15	A34		A36	D34		
C3_A14	A35		A34	D35		
C3_A13	A36		A35	D36		
C3_A12	A37	10	A37	D37		
C3_A11	A38		A40	D38		
C3_A10	A39		A38	D39		
C3_A9	A40		A39	D40		
C3_A8	A41	11	A41	D41	mcm # 12: D47 & D48, D45 & D46 mcm # 11: D43 & D44, D41 & D42	F/f
C3_A7	A42		A44	D42		
C3_A6	A43		A42	D43		
C3_A5	A44		A43	D44		
C3_A4	A45	12	A45	D45		
C3_A3	A46		A48	D46		
C3_A2	A47		A46	D47		
C3_A1	A48		A47	D48		
C4_A16	A49	13	A49	D49	mcm # 13: D51 & D52, D49 & D50 mcm # 14: D55 & D56, D53 & D54	G/g
C4_A15	A50		A52	D50		
C4_A14	A51		A50	D51		
C4_A13	A52		A51	D52		
C4_A12	A53	14	A53	D53		
C4_A11	A54		A56	D54		
C4_A10	A55		A54	D55		
C4_A9	A56		A55	D56		
C4_A8	A57	15	A57	D57	mcm # 16: D63 & D64, D61 & D62 mcm # 15: D59 & D60, D57 & D58	H/h
C4_A7	A58		A60	D58		
C4_A6	A59		A58	D59		
C4_A5	A60		A59	D60		
C4_A4	A61	16	A61	D61		
C4_A3	A62		A64	D62		
C4_A2	A63		A62	D63		
C4_A1	A64		A63	D64		
					mcm # 16: D63 & D64, D61 & D62 mcm # 15: D59 & D60, D57 & D58	V/v

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Table 3: PPM channel mapping for JEM LVDS links, for channels 1 to 32, corresponding to the upper two analogue connectors on the front panel. The fanout links contain other channels as well. C: Connector; FP: Front Panel; BP: Back Plane.

Analog C ch#	Analog FP ch#	MCM slot #	MCM ch map	Digital ch#	PPM to JEM LVDS Connector	PPM/JEM BP		
					MCM # 5 / MCM # 16			F1/f1
					MCM # 9 / MCM # 4			F2/f2
					MCM # 8		V8/v8	
					MCM # 3 / MCM # 4 / MCM # 2 / MCM # 1	WX/wx	WX/wx	
C1_A16	A1	1	A1	D1	MCM # 3 / MCM # 4 / MCM # 2 / MCM # 1	AB/ab	AD/ad	AH/ah
C1_A15	A2		A4	D2				
C1_A14	A3		A2	D3				
C1_A13	A4		A3	D4				
C1_A12	A5	2	A5	D5				
C1_A11	A6		A8	D6				
C1_A10	A7		A6	D7				
C1_A9	A8		A7	D8				
C1_A8	A9	3	A9	D9				
C1_A7	A10		A12	D10				
C1_A6	A11		A10	D11				
C1_A5	A12		A11	D12				
C1_A4	A13	4	A13	D13				
C1_A3	A14		A16	D14				
C1_A2	A15		A14	D15				
C1_A1	A16		A15	D16				
C2_A16	A17	5	A17	D17	MCM # 7 / MCM # 8 / MCM # 6 / MCM # 5	CD/cd	EH/eh	AH/ah
C2_A15	A18		A20	D18				
C2_A14	A19		A18	D19				
C2_A13	A20		A19	D20				
C2_A12	A21	6	A21	D21				
C2_A11	A22		A24	D22				
C2_A10	A23		A22	D23				
C2_A9	A24		A23	D24				
C2_A8	A25	7	A25	D25				
C2_A7	A26		A28	D26				
C2_A6	A27		A26	D27				
C2_A5	A28		A27	D28				
C2_A4	A29	8	A29	D29				
C2_A3	A30		A32	D30				
C2_A2	A31		A30	D31				
C2_A1	A32		A31	D32				

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Table 4: PPM channel mapping for JEM LVDS links, for channels 33 to 64, corresponding to the lower two analogue connectors on the front panel. The fanout links contain other channels as well. C: Connector; FP: Front Panel; BP: Back Plane.

Analog C ch#	Analog FP ch#	MCM slot #	MCM ch map	Digital ch#	PPM to JEM LVDS Connector	PPM/JEM BP		
C3_A16	A33	9	A33	D33	MCM # 11 / MCM # 12 / MCM # 10 / MCM # 9	EF/ef	AD/ed	AH/ah
C3_A15	A34		A36	D34				
C3_A14	A35		A34	D35				
C3_A13	A36		A35	D36				
C3_A12	A37	10	A37	D37				
C3_A11	A38		A40	D38				
C3_A10	A39		A38	D39				
C3_A9	A40		A39	D40				
C3_A8	A41	11	A41	D41				
C3_A7	A42		A44	D42				
C3_A6	A43		A42	D43				
C3_A5	A44		A43	D44				
C3_A4	A45	12	A45	D45				
C3_A3	A46		A48	D46				
C3_A2	A47		A46	D47				
C3_A1	A48		A47	D48				
C4_A16	A49	13	A49	D49	MCM # 15 / MCM # 16 / MCM # 14 / MCM # 13	GH/gh	EH/eh	AH/ah
C4_A15	A50		A52	D50				
C4_A14	A51		A50	D51				
C4_A13	A52		A51	D52				
C4_A12	A53	14	A53	D53				
C4_A11	A54		A56	D54				
C4_A10	A55		A54	D55				
C4_A9	A56		A55	D56				
C4_A8	A57	15	A57	D57				
C4_A7	A58		A60	D58				
C4_A6	A59		A58	D59				
C4_A5	A60		A59	D60				
C4_A4	A61	16	A61	D61				
C4_A3	A62		A64	D62				
C4_A2	A63		A62	D63				
C4_A1	A64		A63	D64				
					MCM # 15 / MCM # 16	VJ/vj	VJ/vj	
					MCM # 10 / MCM # 9		W8/w8	
					MCM # 13 / MCM # 8			F3/f3
					MCM # 1 / MCM # 12			F4/f4

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References

[1] Stephen Hillier, Murrough Landon, *Level-1 Calorimeter Trigger: Cable Mapping and Crate Layouts from Analogue Inputs to Processors,* (ATL-DA-ES-0036, 2005). https://edms.cern.ch/document/399348