STR7200

32 Channel VME Scaler

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1 STR7200 INTRODUCTION **5**

2 BOARD PROPERTIES **6**

2.1 BOARD DESCRIPTION 6
2.2 BLOCK DIAGRAM 7

3 GETTING STARTED **8**

4 VME ACCESS **8**

4.1 ADDRESSING MODES AND BASE ADDRESS 8
4.1.1 ADDRESS MODIFIER OVERVIEW *8*
4.2 ADDRESS MAP 9
4.3 BROADCAST ADDRESSING 9
4.4 DATA WIDTH 10
4.5 READOUT SPEED CONSIDERATIONS 11
4.5.1 BLOCK READS *11*
4.5.2 SINGLE CYCLE READS *11*

5 VME INTERRUPTS (IRQ) **11**

6 REGISTER DESCRIPTION **12**

6.1 STATUS AND CONTROL REGISTER (OFFSET 0) 12
6.1.1 STATUS REGISTER (READ) *12*
6.1.2 Control register (write) *13*
6.2 VME IRQ AND VERSION REGISTER (OFFSET 4) 14
6.3 COUNT DISABLE REGISTER: 14
6.4 COUNTER READ REGISTERS: 15
6.5 COUNTER OVERFLOW REGISTERS: 15
6.6 KEY ADDRESSES 15
6.7 BROADCAST KEY ADDRESSES 15

7 LEDS **16**

8 SIGNAL SPECIFICATIONS **16**

8.1 SCALER INPUTS 16
8.2 CONTROL INPUTS 16

9 POWER CONSUMPTION **17**

10 HARDWARE CONFIGURATION **17**

10.1 JUMPER AND ROTARY SWITCH LOCATIONS 17
10.1.1 LCA DESIGN SELECTION *17*
10.1.2 VME SYSRESET BEHAVIOUR *18*
10.2 INPUT CONFIGURATION 18
10.3 INPUT TERMINATION ON ECL UNITS 18

11 FACTORY DEFAULT SETTINGS **18**

12 SOFTWARE SUPPORT **18**

13 APPENDIX **19**

13.1 FRONT PANEL LAYOUTS 19
13.2 FLAT CABLE CONNECTOR PIN ASSIGNMENTS 20
13.3 CONTROL CONNECTOR 20
13.4 DATA CONNECTOR 20
13.5 BOARD LAYOUT (RESISTOR NETWORK LOCATIONS) 21
13.6 INPUT CONFIGURATION 22
13.6.1 Control Inputs *22*

13.6.2 Scaler Inputs *23*
13.7 EPROM VERSION(S) AND LCA FILES 24

1 STR7200 INTRODUCTION

The STR7200 is a versatile single slot (flat cable version) or two slot wide (LEMO version) 6U VME 32 channel scaler with 32 bits counting depth. The ECL and NIM versions can count frequencies up to 200 MHz and the TTL version 100 MHz. A total of 8 control inputs and outputs (inputs only are supported by design 1 version 1 of the STR7200) allow for an easy integration into readout systems with a wide range of demands. By the use of LCA (logic cell array) technique it was possible to implement a great deal of flexibility. Up to 8 different LCA designs can be selected by the means of jumpers, the STR7200 in its classic scaler form being the first implementation, a multiscaler (STR7201), a prescaler (STR7202) and a latch (STR7137) are possible future designs. Another possible design to mention in this context is a 16 channel 64 bit deep scaler. The LCA designs are loaded from an upgraded boot EPROM. The latest revision of this EPROM will be available at an attractive upgrade fee. Send an email to support@struck.de to become included into the mailing list of STR7200 users. An optional FIFO (1k to 64 k depth) is yet another way to head for the greatest possible flexibility. Broadcast capabilities facilitate and enhance the use in multi unit setups. Special care was taken to get a cost effective unit (+5 V only are required from VME, -5.2 V are generated by a DC/DC converter eg.) and to have an easy getting started setup to see the unit acquiring counts after a minimum initialisation.
This manual describes design 1 version 1 of the STR7200. A list of available EPROM versions and their LCA files can be obtained from http://www.struck.de/720xlca.htm.

2 BOARD PROPERTIES

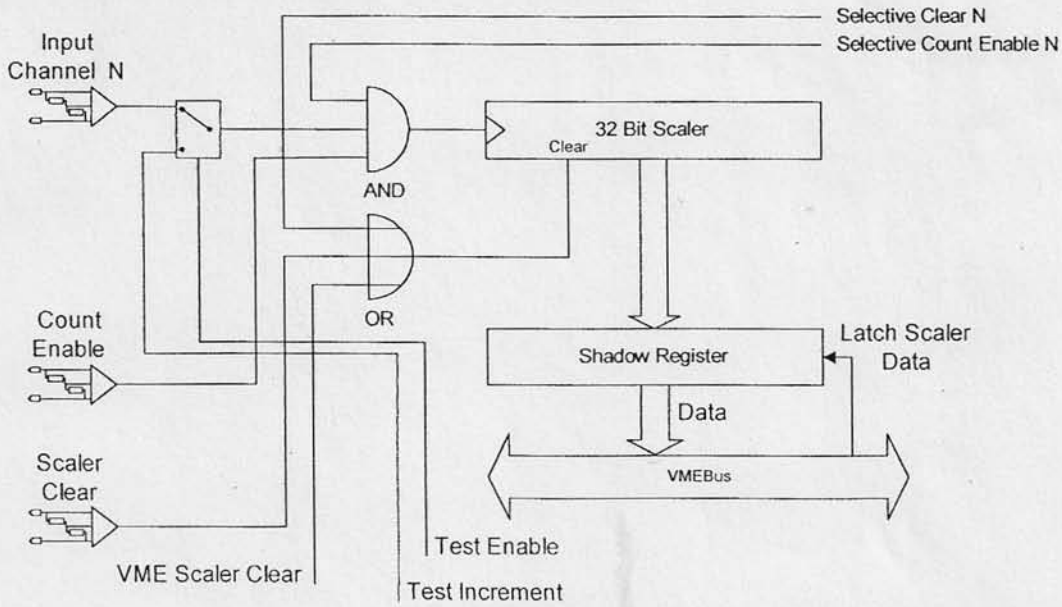
2.1 BOARD DESCRIPTION

The board consists of four groups of 8 scaler channels and one group of 8 control in/outputs. The input levels can be set to NIM, ECL or TTL in groups of 4 channels (from the electric point of view), the outputs can drive NIM or ECL. Input termination can be removed in the ECL case (refer to chapter 10.3) to allow for daisy chaining with other units. Control in/outputs can be assigned in groups of 4 channels. LEMO or flat cable connectors are available.

The main board properties are:

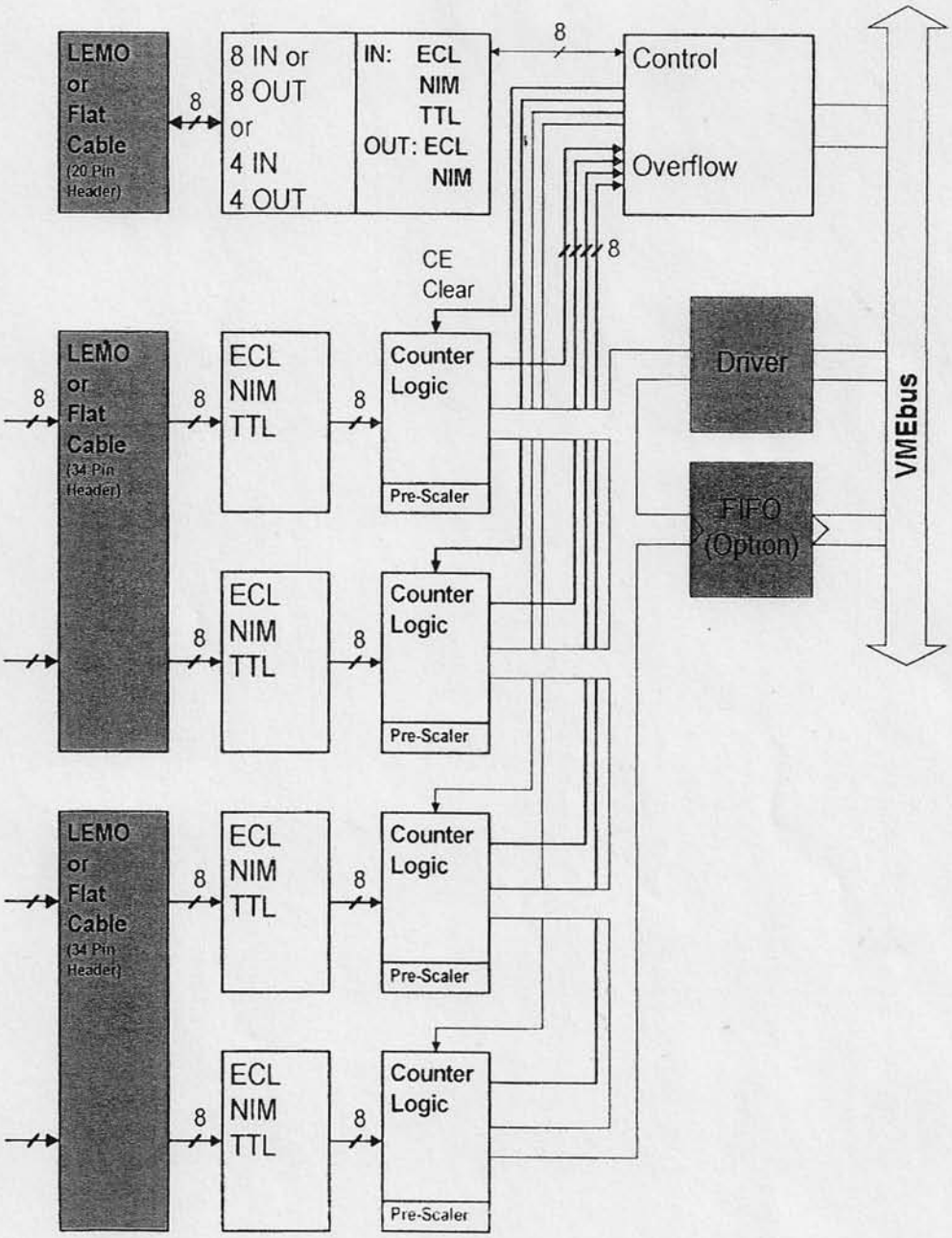
- 32 scaler channels
- Up to 200 MHz input rate (ECL)
- 32-bit channel range (16 channel, 64 bit version available on request)
- Up counter without preset
- Read on the fly
- Count enable by soft and hardware
- Scaler clear by soft and hardware (selective or global)
- Overflow Interrupt capability
- Continuous count
- Shadow register
- External shadow latch input
- Built in test
- Broadcast addressing
- Optional FIFO

The diagram below shows the count enable and clear logic



2.2 BLOCK DIAGRAM

The block diagram illustrates the basic components of the STR7200.



3 GETTING STARTED

The easiest operating mode of the STR7200 requires no external cabling besides the scaler inputs. It consists in a block read of the 32 channels from the key address OFFSET+0x300 after setting up the address modifier (AM) and data width. The access to this address inhibits counting, latches the scaler contents to the shadow register, clears all scaler channels and enables counting. During the latching phase the unit is not acquiring new counts for some 200 ns. Counting has to be enabled by a write to OFFSET+0x28 (global count enable register). This mode is probably all you need for many laboratory or test beam applications.

Note: Crate power has to be off during installation and removal of the unit.

The factory default settings of the unit are described in chapter 11 (Factory default settings).

The selection of the addressing mode (A16, A24 or A32), and the data width is described in the following section VME access.

Example C code, which is enclosed with shipments of STR7200s, gives an overview on how to utilise the different capabilities of the unit.

4 VME ACCESS

The VME access LED (SEL) gives you an easy way to verify, that you are properly accessing the VME slave port of the STR7200.

4.1 ADDRESSING MODES AND BASE ADDRESS

The STR7200 supports short (A16), standard (A24) extended addressing (A32). In all three modes the unit responds to user and supervisory access. The unit occupies 2 KB of the VME address space.

Depending on the selected address mode (Jumpers EN_A32, EN_A24 and EN_A16) the 4 rotary switches SW_A32U, SW_A32L, SW_A24 and SW_A16 and the jumper J_A11 are used to set the base address. Bit 11 is used for the address decoding independent of the rotary switch settings (ie. with J_A11 open bit 11 of the address has to be set, with J_A11 closed it has to be cleared). With the jumper EN_A32 set the setting on the two rotary switches SW_A32U and SW_A32L is evaluated, with the jumper EN_A24 the setting of the rotary switch SW_A24 is evaluated and with the jumper EN_A16 set the setting of the rotary switch SW_A16 is evaluated.

4.1.1 ADDRESS MODIFIER OVERVIEW

The table below gives a complete overview on the possible address modifiers.

AM Code hex.	Function
0F	A32 supervisory block transfer (BLT)
0D	A32 supervisory data access
0B	A32 non-privileged block transfer (BLT)
09	A32 non privileged data access
3F	A24 supervisory block transfer (BLT)
3D	A24 supervisory data access
3B	A24 non privileged block transfer (BLT)
39	A24 non-privileged data access
2D	A16 supervisory access
29	A16 non-privileged access

4.2 ADDRESS MAP

Offset	Function
0	Status register (read)/Control register (write)
4	VME IRQ and version register
C	Count disable register
14	reset FIFO (optional)
18	write shadow to FIFO (optional)
20	clear all counter and overflow bits
24	clock shadow register
28	global count enable
2C	global count disable
30	Broadcast; clear all counter and overflow bits
34	Broadcast; clock shadow register
38	Broadcast; global count enable
3C	Broadcast; global count disable
40	clear counter group and overflow channel 1-8
44	clear counter group and overflow channel 9-16
48	clear counter group and overflow channel 17-24
4C	clear counter group and overflow channel 25-32
60	Reset register (KEY_RESET)
68	Test clock (generates one clock)
80	read FIFO (optional)
100-17C	clear counter x and ist overflow bit
180-1FC	clear overflow bit of counter x
200-27C	read shadow register
280-2FC	read counter
300-37C	read and clear all counters
380	Overflow register channel 8-1
3A0	Overflow register channel 16-9
3C0	Overflow register channel 24-17
3E0	Overflow register channel 32-25

4.3 BROADCAST ADDRESSING

addressing mode can be used with the A32 or A24 addressing mode enabled, when the bit enable broadcast (bit 6 of control register) is set on all units which are supposed to participate in the cycle and the bit enable broadcast handshake (bit 7 of control register) is set on one of the units. To make use of broadcasting the A32 and A24 address portion of the participating STR7200s must be set to the identical value if A32 addressing is used, with A24 addressing the A24 setting must be identical. The A32/A24 part of the address can be seen as kind of a broadcast class. The distinction of the scalers in one broadcast class is made by their SW_A16 and J_A11 setting. An A32 access to a broadcast key address (0x30 eg.) with the A32 and A24 address offset of the class will access all units of this class eg.

NOTE: Let the 32 bit address be denoted as 8 nibbles x1 x2 y1 y2 z z z z (the z portion is ignored in broadcast addressing). No (non STR7200) units with the same x1, x2, y1, y2 section are allowed in the crate with A32 addressing, no units with the same y1, y2 section in the case of A24 addressing.

Broadcast Example 1: 3 STR7200 participating in broadcast, A32
EN_A32 jumper set on all units.
Set the base addresses like in the following table:

Unit	Base address setting
1	0x33501000
2	0x33502000
3	0x33503000

Enable Broadcast on all units by setting bit 6 of the control register.
Enable Broadcast handshake on one unit, set bit 7 of control register of unit 1.
An A32 write to address 0x33500030 will clear all counters and overflow bits on units 1 to 3.

Broadcast Example 2: 4 STR7200 participating in broadcast, A24
EN_A24 jumper set on all units.
Set the base addresses like in the following table:

Unit	Base address setting
1	0x701000
2	0x701800
3	0x702000
4	0x702800

Enable Broadcast on all units by setting bit 6 of the control register.
Enable Broadcast handshake on one unit, set bit 7 of control register of unit 4.
An A24 write to address 0x700038 will enable counting on units 1 to 4.

Note: Transactions executed via a broadcast cycle result in a worst case jitter of 40 ns

4.4 DATA WIDTH

The STR7200 can be accessed with 16 bit (D16) and 32 bit (D32) data. Block transfer (BLT32) is also implemented. For the sake of overall system performance we recommend the use of D32 or even better BLT32, if this mode is supported by your VME master. Refer to your VME masters documentation for a description on how to set the data transfer width and to enable block transfer mode.

4.5 READOUT SPEED CONSIDERATIONS

4.5.1 BLOCK READS

A readout speed of 220 ns/32 bit word was measured with a STR8080 as VME master accessing the STR7200 in block mode (BLT32), corresponding to some 18 MB/s. The slave timing (DS01.L to DTACK) contribution from the STR7200 is 80 ns (for the second and following words of the transfer).

4.5.2 SINGLE CYCLE READS

If your CPU does not support block reads or you can't use them for other reasons, you can minimise readout time by keeping in mind the architecture of the STR7200 and utilising the characteristics. Scaler reads are performed by the hardware in two steps. First the scaler contents is copied into the shadow register, then the data from the shadow register are available for the VME bus. As the contents of all 32 channels is copied to the shadow registers on any counter read you can save the time needed for the copy process by reading the first counter directly only (0x280) and reading the contents of the other counters from the shadow registers (0x204-0x27C). An additional advantage of doing so, is that the scaler contents are copied within a period of some 200 ns and the resulting error from the readout phase is thus minimised in the absence of external disable circuitry.

5 VME INTERRUPTS (IRQ)

Four interrupt sources are implemented (Overflow, External (Latch Shadow Control Input), FIFO full (optional), FIFO half full (optional)). The generation of interrupts is enabled by setting bit 11 of the VME IRQ and Version register, the various interrupt sources are enabled by writing a one into the corresponding bit of the Control Register and disabled by writing a one into the corresponding disable bit. The VME interrupt level is defined by bits 8 through 10 of the VME IRQ and Version Register. The VME IRQ interrupt vector has to be written into bits 0 through 7 of the VME IRQ and Version Register.
In general the interrupt condition is cleared by disabling and enabling the corresponding interrupt, in case of an overflow interrupt the overflow condition has to be cleared by clearing the corresponding Counter Overflow Register in addition.

6 REGISTER DESCRIPTION

The STR7200 occupies 1 KB (ie. the area from the base address until base address +0x3ff) of the VME address space. In the following register description all offsets are given in hexadecimal notation.

6.1 STATUS AND CONTROL REGISTER (OFFSET 0)

6.1.1 STATUS REGISTER (READ)

Bit	Name
31	VME IRQ source 3 (VME_IRQS_3) FIFO full (optional)
30	VME IRQ source 2 (VME_IRQS_2) FIFO half full (optional)
29	VME IRQ source 1 (VME_IRQS_1) External IRQ (ext. clock shadow)
28	VME IRQ source 0 (VME_IRQS_0) Overflow
27	VME_IRQ
26	internal VME_IRQ
25	0
24	0
23	Control bit VME IRQ source 3 FIFO full (optional)
22	Control bit VME IRQ source 2 FIFO half full (optional)
21	Control bit VME IRQ source 1 External IRQ (ext. clock shadow)
20	Control bit VME IRQ source 0 Overflow
19	Control bit reserve
18	Control bit reserve
17	Control bit reserve (FIFO test mode)
16	Control bit reserve (FIFO mode)
15	Global COUNT_ENABLE
14	General Overflow Bit
13	0
12	(FIFO_FLAG FULL)
11	(FIFO_FLAG ALMOST FULL)
10	(FIFO_FLAG HALF FULL)
9	(FIFO_FLAG ALMOST EMPTY)
8	(FIFO_FLAG EMPTY)
7	Control bit broadcast mode handshake controller
6	Control bit broadcast mode
5	Control bit Input Test mode
4	Control bit Testpulses 25MHZ
3	Control bit input mode bit 1
2	Control bit input mode bit 0
1	Control bit reserve
0	Control bit User LED

6.1.2 Control register (write)

The control register is implemented in form of a selective J/K register. A zero written into the corresponding bit has no effect, a 1 written into the enable bit activates the specified function, a 1 written into the disable bit disables the function. Writing a one into both the enable and disable bit results in an undefined toggle state and is thus not allowed.

Bit	Function
23/32	enable/disable IRQ source 3
22/30	enable/disable IRQ source 2
21/29	enable/disable IRQ source 1
20/28	enable/disable IRQ source 0
19/27	set/clr(*) reserve
18/26	set/clr(*) reserve
17/25	reserve (enable/disable(*) FIFO test mode)
16/24	reserve (enable/disable(*) FIFO mode)
7/15	enable/disable(*) broadcast mode handshake controller
6/14	enable/disable(*) broadcast mode
5/13	enable/disable(*) Input Test mode
4/12	enable/disable(*) Test pulses 25 MHz
3/11	set/clr(*) control input mode bit 1
2/10	set/clr(*) control input mode bit 0
1/9	set/clr(*) reserve
0/8	set/clr(*) User LED

* Power on reset or KEY_RESET

Control Input Modes

Mode 0 (bit1=0, bit0=0): all control inputs are disabled

Mode 1 (bit1=0, bit0=1): input 1 -> disables count all channels
input 2 -> clears all channels
input 5 -> shadow reg. clock
input 7 -> external count test pulse (max. 50 MHz)

Mode 2 (bit1=1, bit0=0): input 1 -> disables count channels 1 - 16
input 3 -> disables count channels 17 - 32
input 2 -> clears channels 1 - 16
input 4 -> clears channels 17 - 32
input 5 -> shadow reg. clock
input 7 -> external count test pulse

Mode 3 (bit1=1, bit0=1): input 1 -> disables count channels 1 - 8
input 3 -> disables count channels 9 - 16
input 5 -> disables count channels 17 - 24
input 7 -> disables count channels 25 - 32
input 2 -> clears channels 1 - 9
input 4 -> clears channels 9 - 16
input 6 -> clears channels 17 - 24
input 8 -> clears channels 25 - 32

6.2 VME IRQ AND VERSION REGISTER (OFFSET 4)

This read/write register controls the VME interrupt control logic on the STR7200. It is possible to enable/disable the generation of a VME interrupt if an internal VME_IRQ is set, to determine the VME IRQ Level (IRQ[7..1]) and to determine the 8-bit Status/ID (Interrupt Vector). The type of the Interrupter is **D08(O).**

In addition this register holds the desing number and version number of the selected LCA file of the installed boot EPROM.

Bit	Name	R/W	Function
31	Design number bit 7	read only	
	..	..	Design number = 1 for STR7200
25	Design number bit 0	read only	
24	Version number bit 7	read only	
	..	..	first version = 1
16	Version number bit 0	read only	
15	reserved	read only	"0"
14	reserved	read only	"0"
13	reserved	read only	"0"
12	reserved	read only	"0"
11	VME_IRQ_ENABLE	read/write	"0": VME IRQ is disabled ; "1": VME IRQ is enabled ;
10	VME_IRQ_LEV2	read/write	determines the VME IRQ Level on VME
9	VME_IRQ_LEV1	read/write	determines the VME IRQ Level on VME
8	VME_IRQ_LEV0	read/write	determines the VME IRQ Level on VME
7	Status/ID_bit7	read/write	Status/ID bit 7; placed on D7 during VME IRQ acknowledge cycle
6	Status/ID_bit6	read/write	Status/ID bit 6; placed on D6 during VME IRQ acknowledge cycle
5	Status/ID_bit5	read/write	Status/ID bit 5; placed on D5 during VME IRQ acknowledge cycle
4	Status/ID_bit4	read/write	Status/ID bit 4; placed on D4 during VME IRQ acknowledge cycle
3	Status/ID_bit3	read/write	Status/ID bit 3; placed on D3 during VME IRQ acknowledge cycle
2	Status/ID_bit2	read/write	Status/ID bit 2; placed on D2 during VME IRQ acknowledge cycle
1	Status/ID_bit1	read/write	Status/ID bit 1; placed on D1 during VME IRQ acknowledge cycle
0	Status/ID_bit0	read/write	Status/ID bit 0; placed on D0 during VME IRQ acknowledge cycle

Example for VME IRQ Level 5 (IRQ5): VME_IRQ_LEV2 = 1
VME_IRQ_LEV1 = 0
VME_IRQ_LEV0 = 1

6.3 COUNT DISABLE REGISTER:

Register Offset	Function
C	Count Disable Register (write, 32 bit) if register bit(xx)=1, then channel xx+1 is disabled to count

6.4 COUNTER READ REGISTERS:

Register Offset	Function
200-27C	read shadow register * (D16, D32, BLT32)
280-2FC	read counter ** (D16, D32, BLT32)
300-37C	read and clear all counters (D32, BLT32)

* clock shadow register and read shadow register
**disable count - clock shadow -clear counter - enable counter

6.5 COUNTER OVERFLOW REGISTERS:

Register Offset	Function
380	Overflow register ch. 8 - 1 (ch 8 → Bit 31,.. ch 1 -> Bit 24)
3A0	Overflow register ch. 16 - 9 (ch 16→ Bit 31,.. ch 9 -> Bit 24)
3C0	Overflow register ch. 24 - 17 (ch 24→ Bit 31,.. ch 17-> Bit 24)
3E0	Overflow register ch. 32 - 25 (ch 32→ Bit 31,.. ch 25-> Bit 24)

6.6 KEY ADDRESSES

A write to the following key addresses with arbitrary data starts the execution of the specified function.

Register Offset	Function
20	clear all counter and overflow bits
24	clock shadow register
28	global count enable
2C	global count disable ***
40	clear counter group and overflow ch 1 - 8
44	clear counter group and overflow ch 9 - 16
48	clear counter group and overflow ch 17 - 24
4C	clear counter group and overflow ch 25 - 32
60	Reset register (KEY_RESET)
68	Test clock (generates one clock)

*** NOTE: this is the state after power on or KEY_RESET, ie. counting has to be enabled by writing to OFFSET+0x28

6.7 BROADCAST KEY ADDRESSES

Register Offset	Function
30	clear all counter and overflow bits
34	clock shadow register
38	global count enable
3C	global count disable (*)

(future: not valid in FIFO-Mode → external signal generates „write shadow register to FIFO " command)

Register Offset	Function
100-17c	clear counter x and its overflow bit (100 → x=1, 104 → x=2, .., 17c = x=32)
180-1FC	clear only overflow bit of counter x (100 → x=1, 104 → x=2, .., 17c = x=32)

FIFO: (optional)

Register Offset	Function
80	read fifo (data access, blocktransfer)
10	
14	reset FIFO
18	write shadow register to FIFO (all 32 channels)

7 LEDs

A total of 6 LEDs is implemented on the STR7200. After Power On Reset the LCA Logic will be configured. During this setup time (1 to 2 seconds) all LEDs except the RDY LED are on (LED test). After completion the RDY LED only is on.

RDY	Green; indicates that the STR7200 logic (LCA) is ready.
SEL	Yellow; this LED is lit whenever the STR7200 is accessed from VME
CEN	Green; lit when counting on one or more channels is enabled (independent of state of disable register)
OFL	Green; lit on occurrence of an overflow
CLR	Green; lit when one or more channels are cleared
USR	Red; to be set/cleared under user program control.

8 Signal Specifications

8.1 Scaler Inputs

The minimum signal low and high time is 2.5 ns for ECL and NIM (200 MHz) and 5 ns for TTL (100 MHz) input configuration. For unclean signals (after transmission over long cables eg.) the actual time over the defined high and low level has to be taken into account.
On the ECL version open inputs should be disabled by software.

8.2 Control Inputs

The duration of the clear pulse has to be greater 40 ns, the duration of the latch shadow pulse has to be greater 20 ns. The disable pulse has an internal delay of approximately 20 ns and has to be present for the time you wish to disable counting.
The maximum frequency for the test count input is 50 MHz.

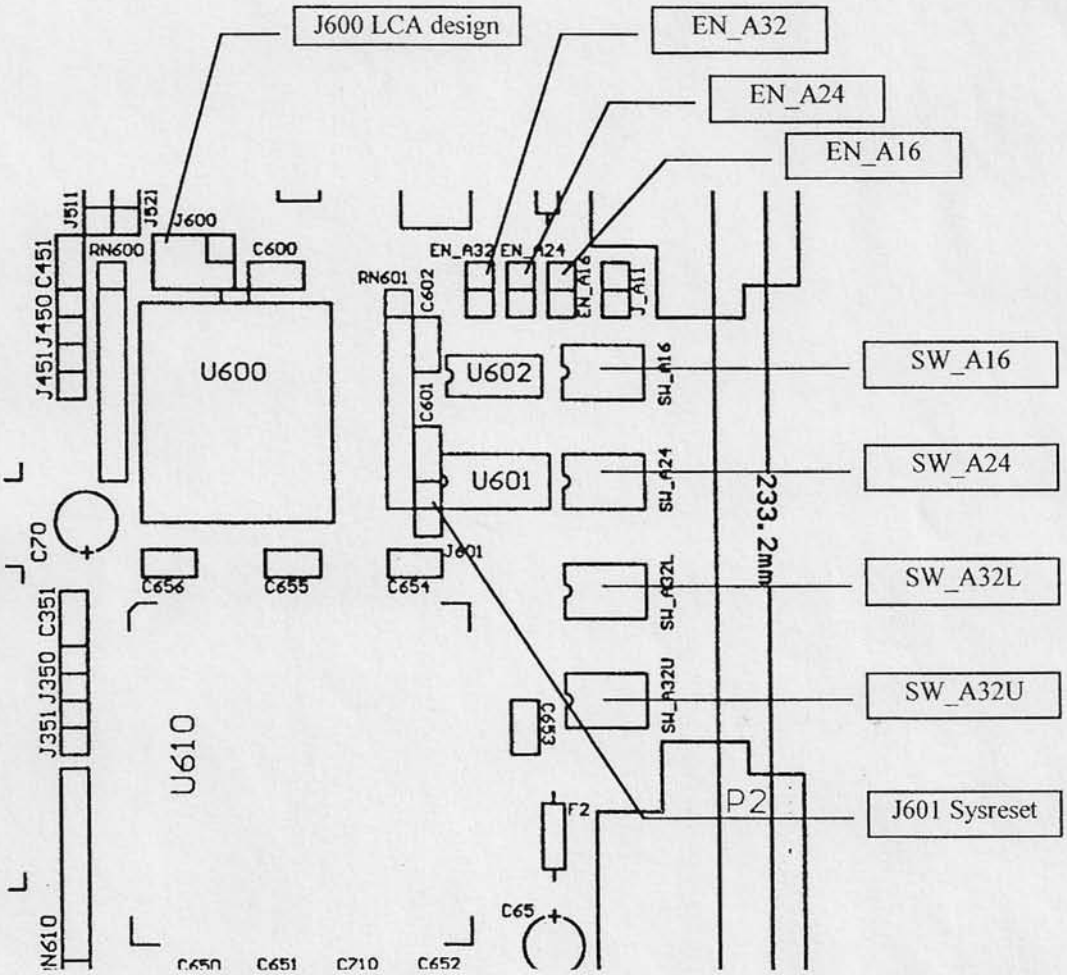
9 POWER CONSUMPTION

The typical power consumption is 15 W (5V, 3A), power consumption at full load (all channels counting at 200 MHz) is 22.5 W (5V, 4.5A).

10 HARDWARE CONFIGURATION

10.1 JUMPER AND ROTARY SWITCH LOCATIONS

The jumper and rotary switch locations are illustrated below, the displayed portion of the board is located on the rear of the board between the P1 and P2 connector.



10.1.1 LCA DESIGN SELECTION

The three bits of jumper field 600 are used to select the LCA file. An open connection refers to a 1, the rightmost jumper pair corresponds to bit 0. In the example below LCA file 1 is selected.

J600

10.1.2 VME SYSRESET BEHAVIOUR

J601 defines the behaviour of the STR7200 upon a Sysreset. With the jumper closed a VME Sysreset will also reset the STR7200 to the power up state (ie. the LCAs are reloaded from the EPROM), with the jumper open Sysreset will be ignored.

10.2 INPUT CONFIGURATION

The inputs of your unit are configured according to your specifications given with the order. In principle the user can modify the input levels in groups of 4 channels to NIM/ECL or TTL. The control and scaler input circuitry is described in chapter 13.6 (Input Configuration).

10.3 INPUT TERMINATION ON ECL UNITS

The input termination on ECL input type STR7200s can be removed in groups of 4 channels by removing the resistor networks listed in the table below.

Input	Networks		
Control Inputs 1-4	RN501	RN511	RN521
Control Inputs 5-8	RN502	RN512	RN522
Inputs 1-4	RN101	RN111	RN121
Inputs 5-8	RN102	RN112	RN122
Inputs 9-12	RN201	RN211	RN221
Inputs 13-16	RN202	RN212	RN222
Inputs 17-20	RN301	RN311	RN321
Inputs 21-24	RN302	RN312	RN322
Inputs 25-28	RN401	RN411	RN421
Inputs 29-32	RN402	RN412	RN422

11 FACTORY DEFAULT SETTINGS

The selected default address mode is A32 (EN_A32 set) with base address 0x33508000. Reset of the STR7200 upon VME Sysreset and LCA file 0 (design 1, version 1 of STR7200) are enabled. On ECL version input termination of 100 Ohms is set.

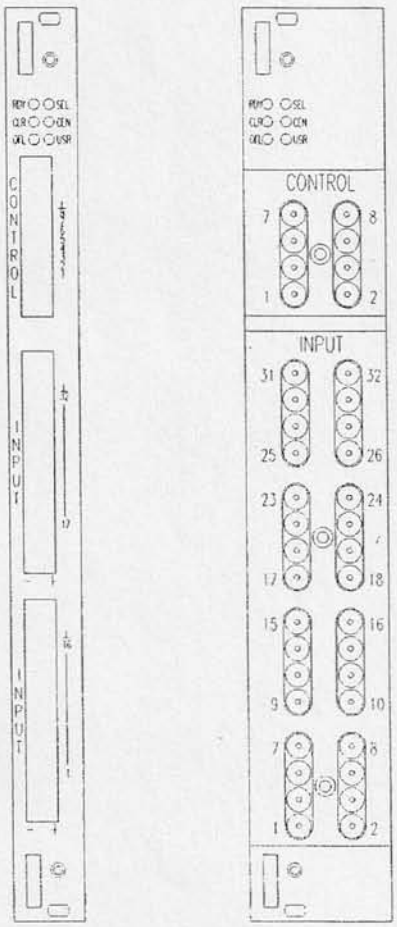
12 SOFTWARE SUPPORT

C example code and header files are included in STR7200 shipments. The code was compiled and run on an ELTEC E6 CPU under OS-9, it is also used to verify the proper function of the units after production. The standard distribution medium is a DOS formatted 3 ½ inch floppy. Send an email to support@struck.de, or contact us via our Web site http://www.struck.de in case of inconvenience with this format, we'll find a way to get the files onto your online system.
Porting the software to other operating systems and platforms should be fairly straightforward, at least as long as no interrupt handling is involved. Drop us a line, if you wish to get system integration support.

13 APPENDIX

13.1 FRONT PANEL LAYOUTS

The following drawing shows the frontpanel layouts of the flat cable (left hand side) and the LEMO version of the STR7200



13.2 Flat Cable Connector Pin Assignments

13.3 Control Connector

The 20-pin header flat cable connector has the following pin assignment:

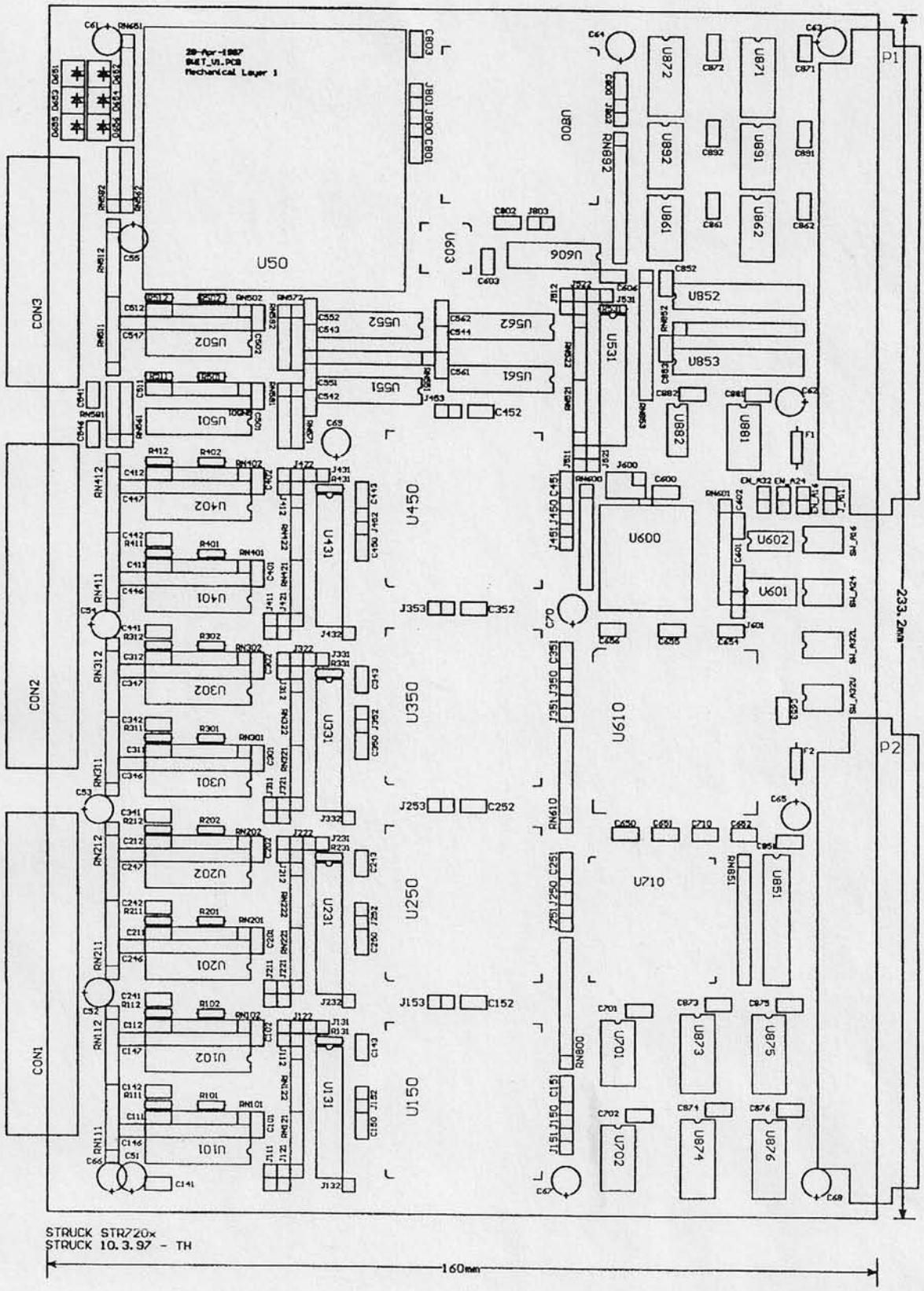
Flat cable:	Pin 20:	GND	Pin 19:	GND
	Pin 18:	-CNTL 8	Pin 17:	+CNTL 8
	Pin 16:	-CNTL 7	Pin 15:	+CNTL 7
	Pin 14:	-CNTL 6	Pin 13:	+CNTL 6
	Pin 12:	-CNTL 5	Pin 11:	+CNTL 5
	Pin 10:	GND	Pin 9:	GND
	Pin 8:	-CNTL 4	Pin 7:	+CNTL 4
	Pin 6:	-CNTL 3	Pin 5:	+CNTL 3
	Pin 4:	-CNTL 2	Pin 3:	+CNTL 2
	Pin 2:	-CNTL 1	Pin 1:	+CNTL 1

13.4 Data Connector

The 34-pin header flat cable connectors have the following pin assignment:

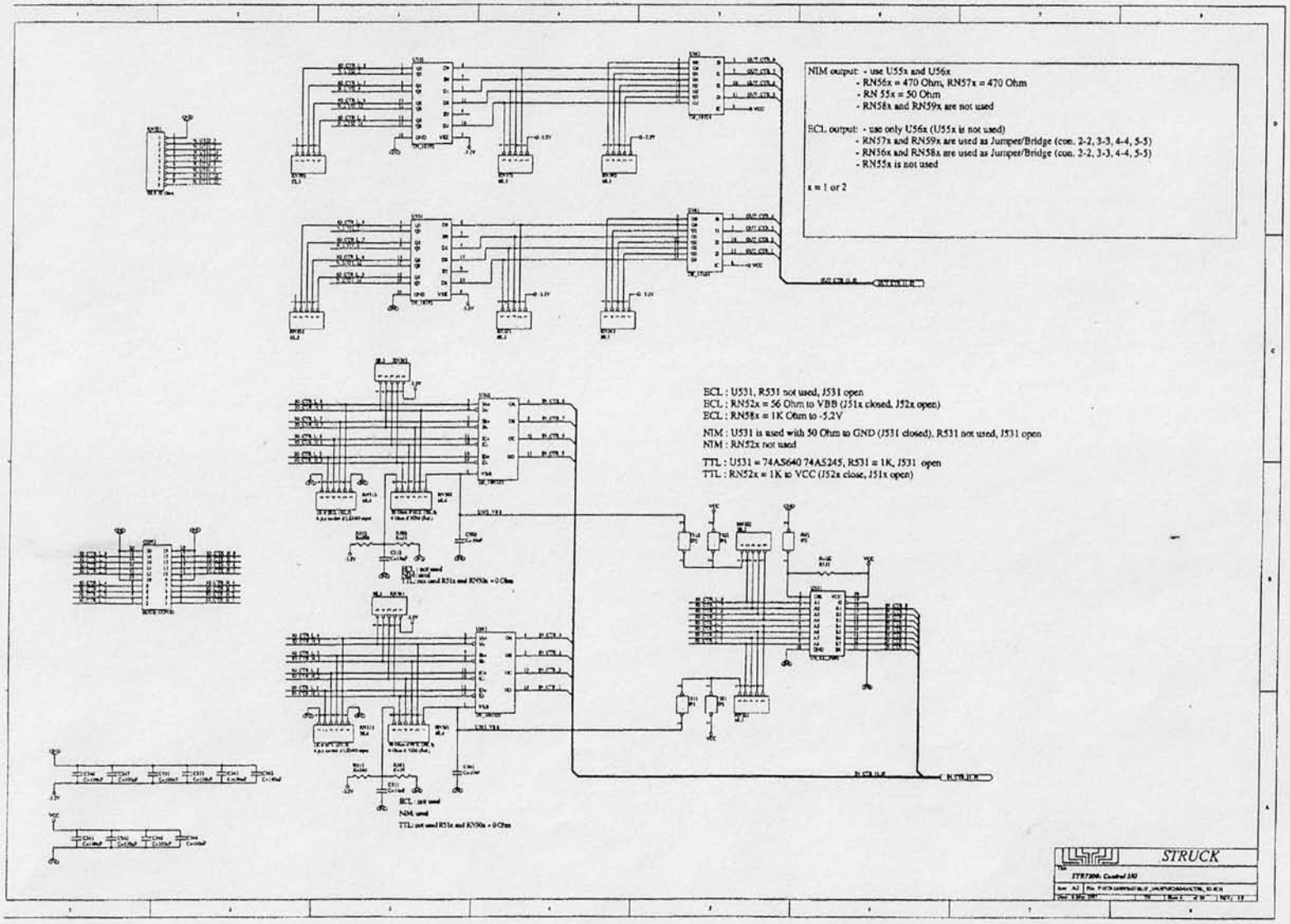
Flat cable:	Pin 34:	GND	Pin 33:	GND
	Pin 32:	-In 16	Pin 31:	+In 16
	Pin 4:	-In 2	Pin 3:	+In 2
	Pin 2:	-In 1	Pin 1:	+In 1

13.5 Board Layout (Resistor Network Locations)

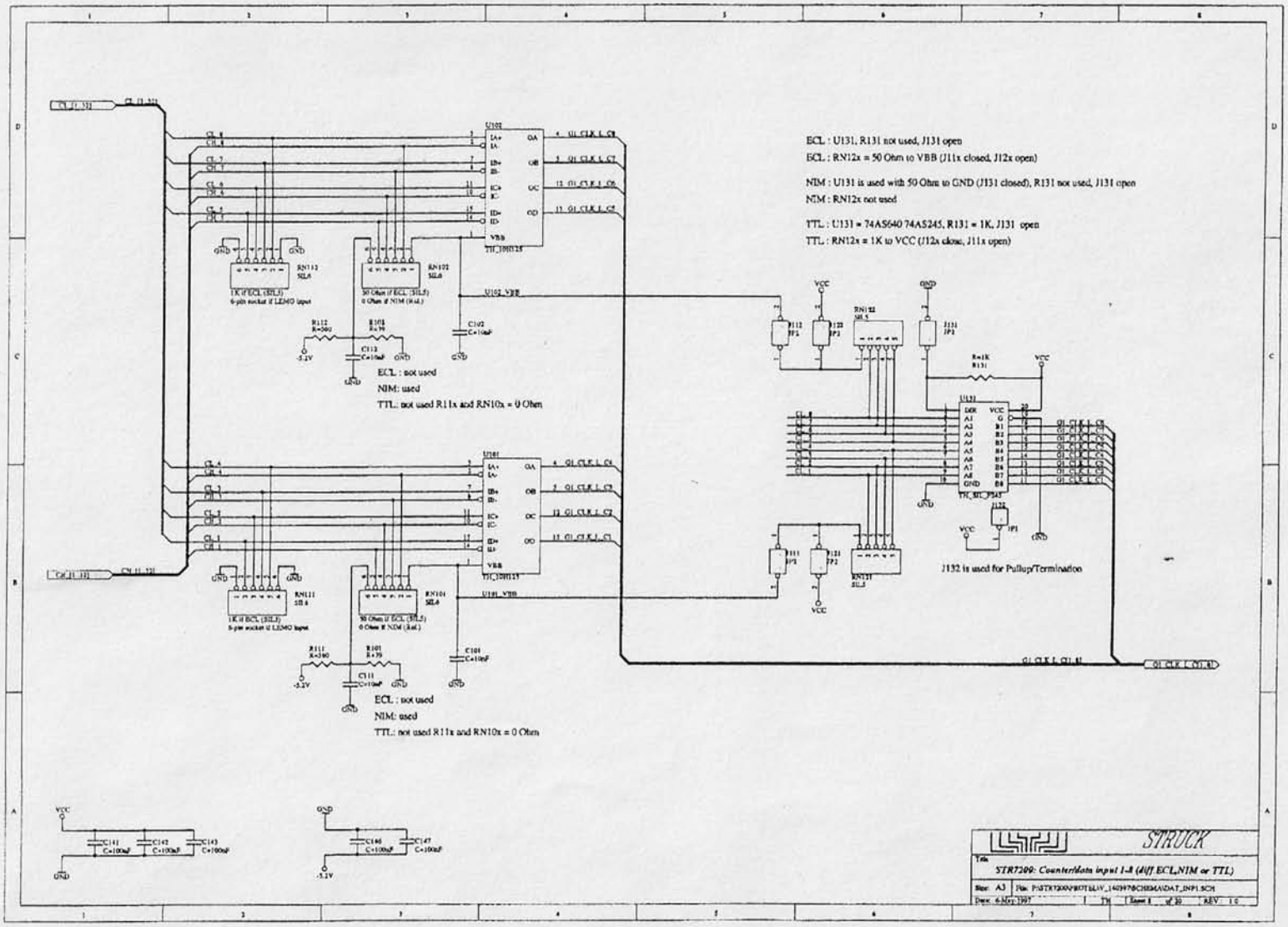


13.6 Input Configuration

13.6.1 Control Inputs



13.6.2 Scaler Inputs



13.7 EPROM VERSION(S) AND LCA FILES

http://www.struck.de/720xlca.htm.

This table has the format:

EPROM name	Designs		
S72_16/97	LCA file	0	STR7200 Design 1 Version 1
		1	-
		2	-
		3	-

At present (6.5.97) the original STR7200 design 1 version 1 is the only available design.