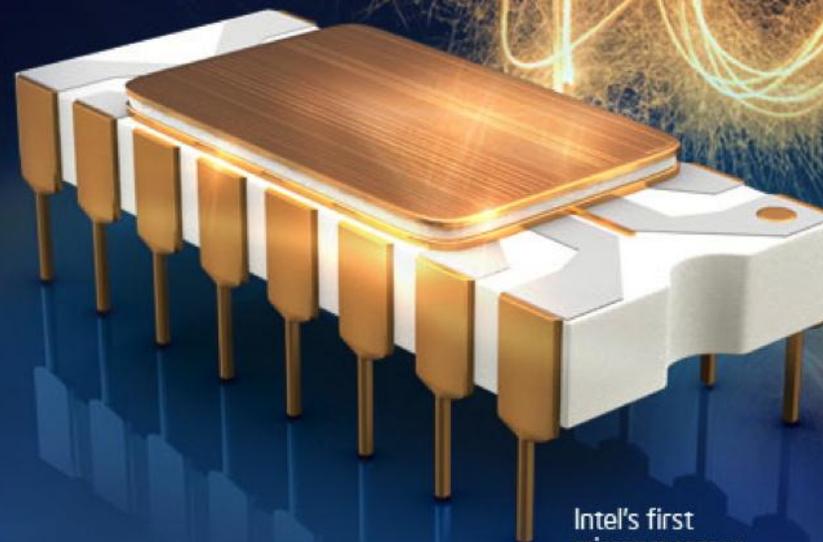


Accelerating HPC

3rd Tracking Workshop, FIAS
February 27th, 2012

Klaus-Dieter Oertel
Intel



Intel's first
microprocessor,
circa 1971.

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Optimization Notice

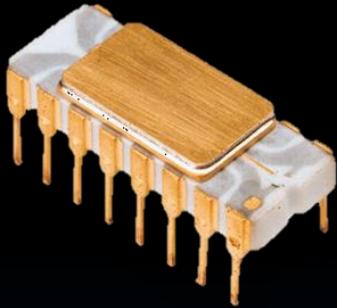
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Notice revision #20101101

40th Anniversary of the Microprocessors



Intel® 4004 (1971)

10000nm, 2300 Transistors
740KHz

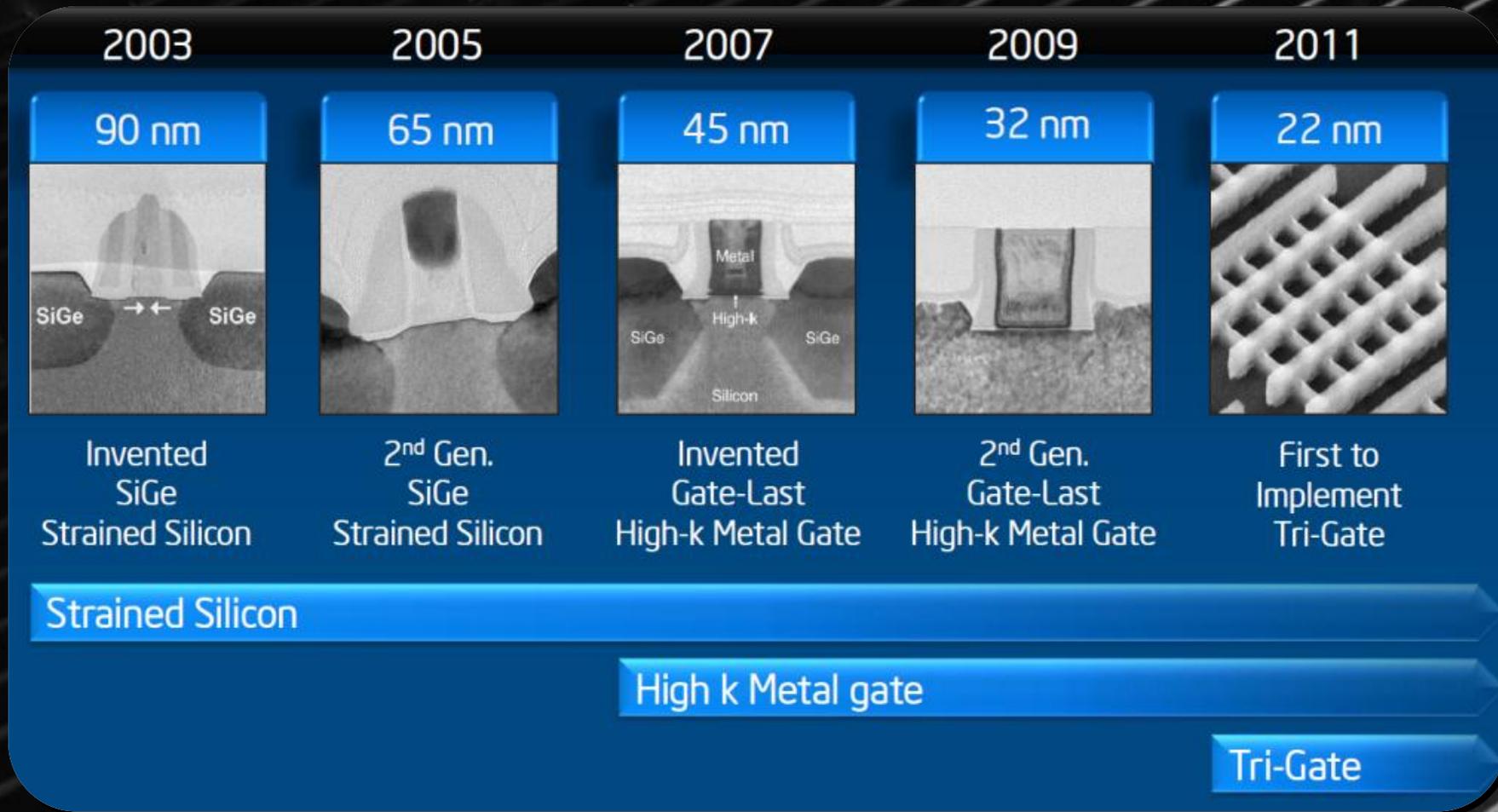


Intel® Core™ i7 (2011)

32nm, 2.27B Transistors
3.6GHz



Transistor Innovations Enable Technology Cadence



22nm

37%
Performance Gain at Low Voltage^[+]

>50%
Active Power Reduction at Constant Performance^[+]

Source: Intel
[+]Compared to Intel 32nm Technology



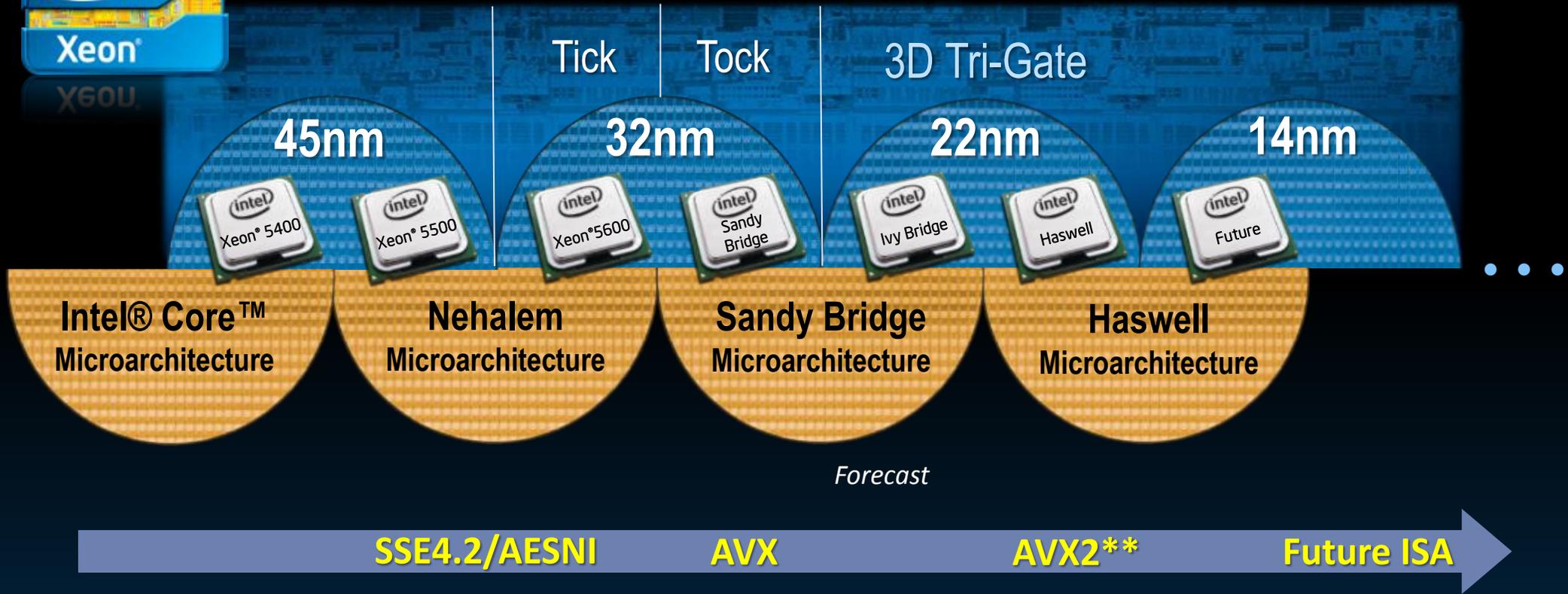
14nm



Well on track

Tick-Tock Development Cycles

Integrate. Innovate.



**Intel® Advanced Vector Extensions Programming Reference, Ref. #319433-011, JUNE 2011

Potential future options, subject to change without notice.



Intel® Xeon® E5 Series Processor

Codename Sandy Bridge-EP

152 GFLOPS DP-F.P. per processor on HPL with 91% efficiency (8C, 2.6GHz)

AVX Instructionset (256-bit SIMD F.P.)

Enhanced Hyper-Threading and Turbo-Technology

Large on-die L3-Cache

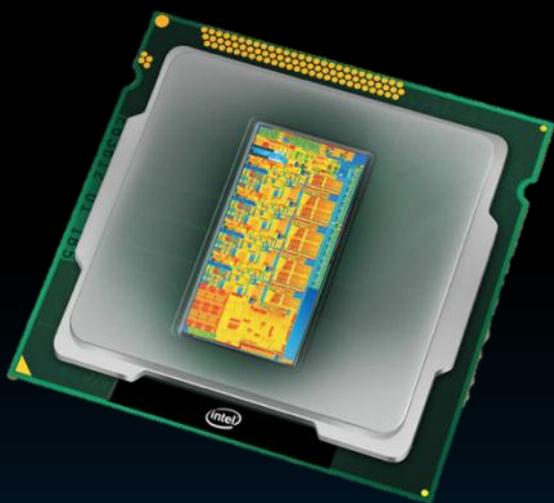
First server processor chip with integrated PCI Express* 3.0 I/O

Early-performance benchmarks**:

- up to 2.1x raw FLOPS (Linpack)
- up to 70% percent more performance using real-HPC workloads
- compared to the previous generation of Intel Xeon 5600 series processors (Westmere)

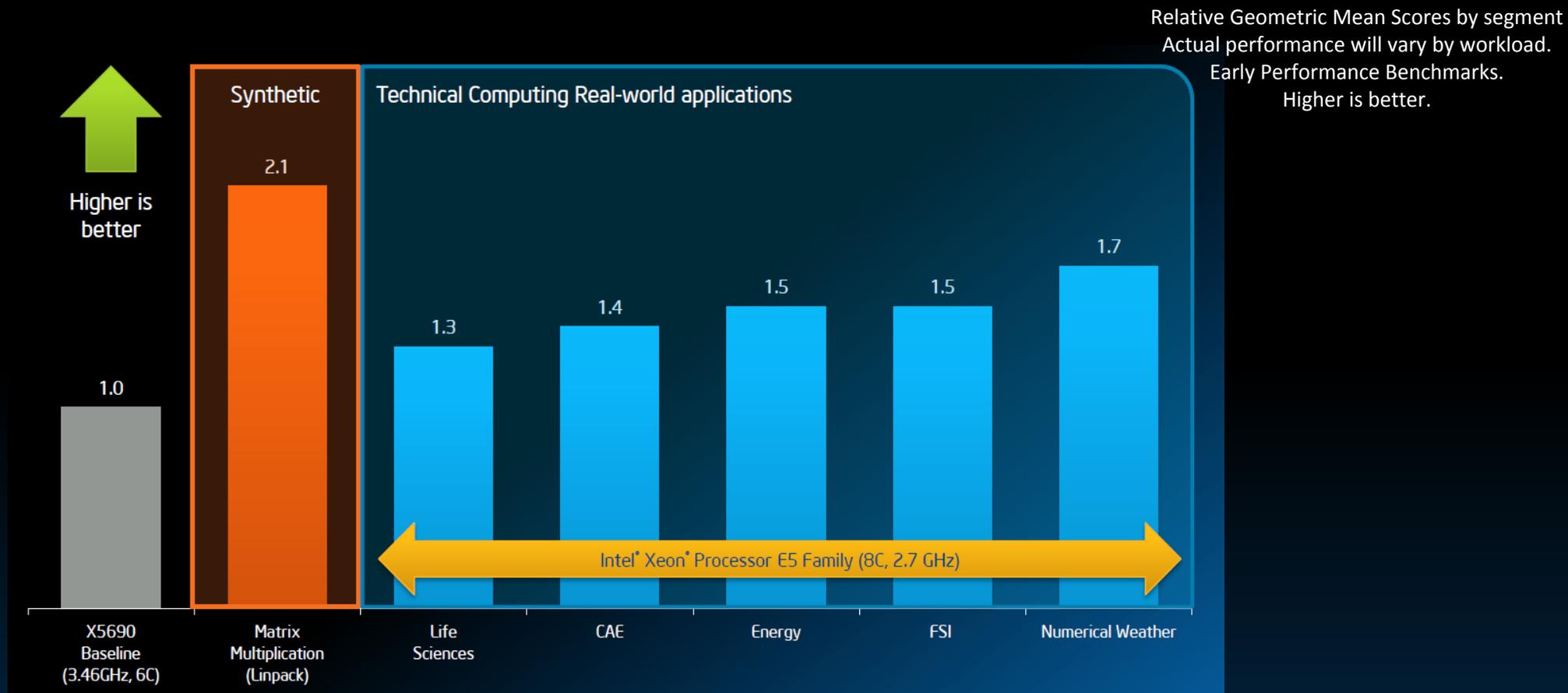
Balanced compute/memory, fast single core/thread multi-core architecture

** Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.



Increased Application Performance

Intel® Xeon® Processor E5 Family



Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. Configurations: Intel Internal measurements October 2011, See backup for configuration details. For more information go to <http://www.intel.com/performance>. Any difference in system hardware or software design or configuration may affect actual performance.

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NCAR selects IBM for key components of new supercomputing center

November 07, 2011

News Release Multimedia Gallery Fact Sheet FAQ More NWSOC News

BOULDER—The National Center for Atmospheric Research (NCAR) today announced that IBM will install critical components of a petascale supercomputing system at the new NCAR-Wyoming Supercomputing Center (NWSOC). The company was selected following a competitive open procurement process.

The IBM components consist of a massive central resource for file and data storage, a high performance computational cluster, and a resource for visualizing the data.

The new system, named Yellowstone, runs on an IBM iDataPlex and is expected to be delivered to the NWSOC early next year. It will be the new facility's inaugural system. Once installed, the system will go through a testing period before being made fully available for scientific research in the summer of 2012.

Yellowstone is expected to deliver 1.6 petaflops performance, or nearly 30 times the capacity of the system currently in use at NCAR's Mesa Laboratory in Boulder, known as bluefire. Petaflops refers to a machine's ability to perform one quadrillion calculations, called floating point operations (FLOPS), per second.

Scientists will use these advanced computing resources to study atmosphere and throughout the Earth system, and to access weather, geomagnetic storms, carbon sequestration, aviation geoscience topics.

The building housing the NCAR-Wyoming Supercomputing Center in Cheyenne, Wyoming, was completed in the summer of 2011. (@UCAR. Photo by Carlye Calvin. This image is freely available for media use. For more information, see [Media & nonprofit use.](#))

“Yellowstone”

- 1.6 PFLOPS peak
- 74592 processor cores
- 149 TB memory
- 17 PB storage
- Deployment scheduled in H1'2012
- IBM* iDataPlex* System
- Intel® Xeon® E5 (Sandy Bridge-EP) processors
- Mellanox* FDR InfiniBand *(56Gb/s) cluster fabric

Intel in High-Performance Computing



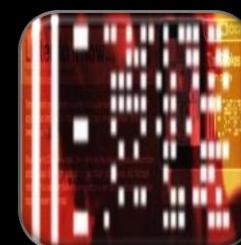
Dedicated,
Renowned
Applications
Expertise



Large Scale
Clusters
for Test &
Optimization



Tera-
Scale
Research



Exa-Scale
Labs



Defined
HPC
Application
Platform



Broad
Software
Tools
Portfolio



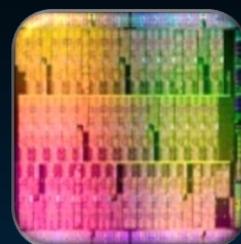
Industry
Standards



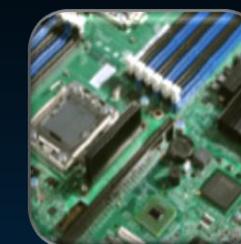
Manufacturing
Process
Technologies



Leading
Processor
Performance,
Energy Efficiency



Many
Integrated
Core (MIC)
Architecture



Platform
Building
Blocks

A long term commitment to the HPC market segment



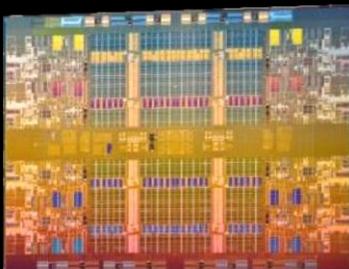
INTEL® MANY INTEGRATED CORE (MIC) ARCHITECTURE

GENERAL PURPOSE ENERGY EFFICIENT
TFLOPS PERFORMANCE
FOR HIGHLY PARALLEL WORKLOAD

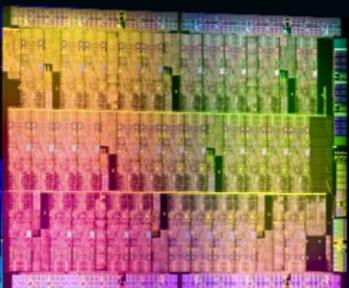
USING COMMON X86 PROGRAMMING MODELS AND SW-TOOLS



Intel's Multi-Core and Many-Core Engines



Multi-core Intel® Xeon® processor up to 3.6 GHz



Many Integrated Cores at 1+ GHz

Intel® Xeon® Processor

- Foundation of HPC Performance
- Suited for full scope of workloads
- Industry leading performance/watt for serial & parallel workloads
- Focus on fast single core/thread performance with “moderate” number of cores

Intel® MIC Architecture

- Optimized for highly parallelized compute intensive workloads
- Common software tools with Xeon enabling efficient application readiness and performance tuning
- IA extension to Many-Core
- Lots of cores/threads with wide SIMD

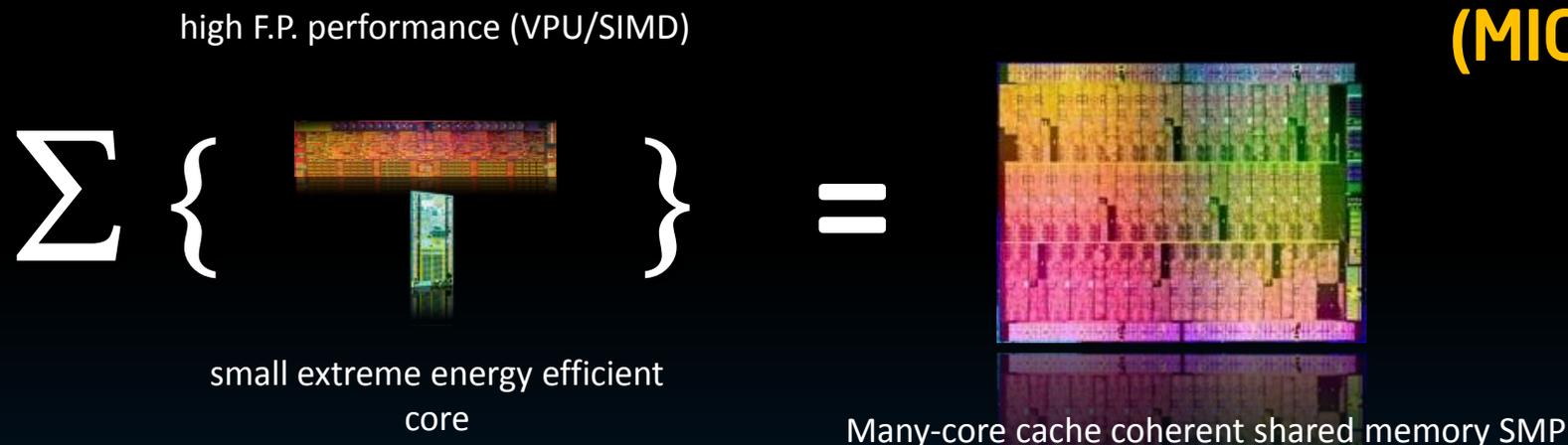
(die-sizes not to scale)



High Performance and Energy Efficiency

for highly Parallel Workloads

Intel® Many Integrated Core (MIC) Architecture



The Newest Addition to the Intel Server Family.
Industry's First General Purpose Many Core Co-Processor Architecture



The “Knights” Family

Future Knights
Products

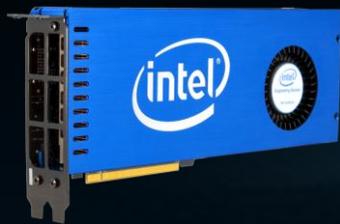


Knights Corner

- 1st Intel® MIC product
- 22nm process
- >50 Intel Architecture cores
- TFLOPS of Performance
- Energy Efficient
- Offload Co-Processor and
- Native Linux* Node Programming

Knights Ferry

Development Platform



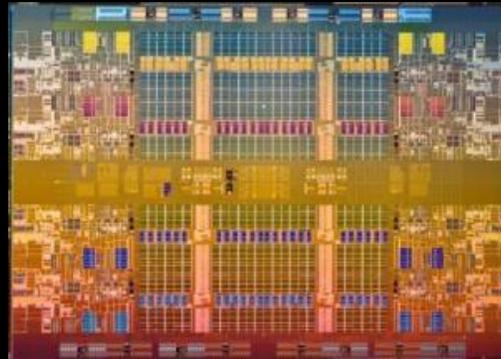
“Programmed like a computer”

All dates, product descriptions, availability, and plans are forecasts and subject to change without notice.

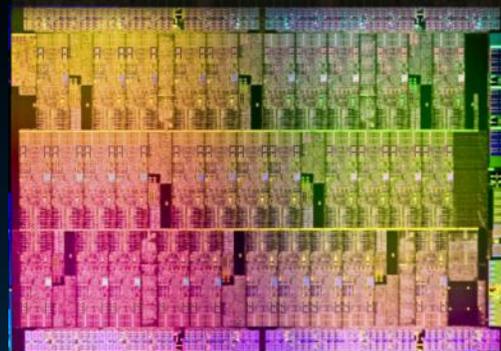
Software Development and System Environment



Same Comprehensive Set
of SW Tools:
Application Source Code
Builds with a
Compiler Switch



Intel® Xeon® Processor



Intel® Many Integrated
Core Architecture

(die-sizes not to scale)

Linux*

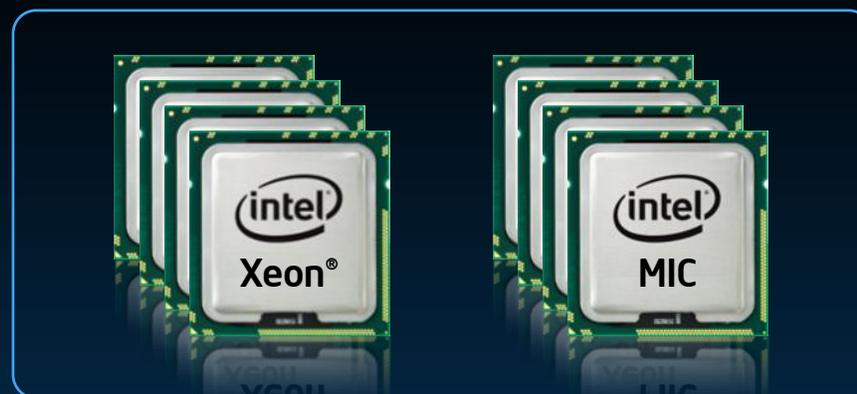


Established HPC
Operating System



Intel Parallel & HPC Programming

Intel® FORTRAN Compiler	Intel® C/C++ Compiler	Intel® Cilk Plus	Intel® Threading Building Blocks	Established Standards	Domain- Specific Libs	Research and Exploration
Fortran Language	C/C++ Language	C/C++ Language Extensions to simply Parallelism Open sourced, Also an Intel product	Widely used C++ Template Library for Parallelism Open sourced, Also an Intel product	MPI Message Passing Co-Array Fortran OpenMP* OpenCL*	Intel® Integrated Performance Primitives (IPP) Intel® Math Kernel Library (MKL)	Intel® Concurrent Collections Offload Extensions Intel® Array Building Blocks Intel® SPMD Parallel Compiler



Experience with Knights Ferry design and development kit



- Unparalleled productivity: in under 3 months
 - Ported all of NWChem (chemistry), ENZO (astro.), ELK (mat. sci.), MADNESS (app. math.), MPI, GA, ...
 - Correct ports in less than one day each
 - Circa 5M LOC (Fortran 77/90, C, C++, Python)
 - MPI, Global Arrays, ...
- Most of this software does not run on GPGPUs and probably never will due to cost and complexity
- Demonstrated execution modes:
 - Native mode: KNF is fully networked Linux system
 - Offload mode: KNF is an attached accelerator
 - Reverse offload mode: KNF in native mode offloads to host
 - Cluster mode: parallel application distributed across multiple KNF and hosts using MPI

NICS

National Institute for Computational Sciences

Joint Institute for Computational Sciences
 University of Tennessee & ORNL



SC'11 November 2011



**1 TFLOPS
DP-F.P.**

(Early Silicon
Demonstration)

MIC: Knights Corner

- In 22nm process technology
- >50 cores/die energy efficient
- 512 bit SIMD instructions
- Early Si delivers 1TFLOPS sustained on DGEMM
- Runs Linux
- Can be
 - a native network node (ssh in ...)
 - used as an offload co-processor
- Common x86 programming models, techniques and tools
- Targeted by Intel compilers and SW-tools
- 3rd party software being enabled



Moore's Law at Work

1997

**1 TFLOPS DP-F.P.
9298 Chips**

“ASCI RED”
~2500 Square Feet
850KW Supercomputer

Source: Sandia

2011

**1 TFLOPS DP-F.P.
Single Chip (MIC)**



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Powering Discoveries That Change The World

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"Stampede's" Comprehensive Capabilities to Bolster U.S. Open Science Computational Resources

Texas Advanced Computing Center's new supercomputer to enable traditional HPC, data-intensive computing, and scientific visualization for nation's scientists

AUSTIN, Texas—The Texas Advanced Computing Center (TACC) at The University of Texas at Austin today announced that it will deploy and support a world-class supercomputer with comprehensive computing and visualization capabilities for the open science community, as part of the National Science Foundation's (NSF) "eXtreme Digital" (XD) program.

The new system, called Stampede, will be built by TACC in partnership with Dell and Intel to support for four years the nation's scientists in addressing the most challenging scientific and engineering problems. NSF is providing \$27.5 million immediately and Stampede is expected to be up and running in January 2013. The estimated investment will be more than \$50 million over four years; the Stampede project may be renewed in 2017, which would enable four additional years of open science research on a successor system.

"Stampede will be one of the most powerful systems in the world and will be uniquely comprehensive in its technological capabilities," said TACC Director Jay Boisseau. "Many researchers will leverage Stampede not only for massive computational calculations, but for all of their scientific computing, including visualization, data analysis, and data-intensive computing. We expect the Stampede system to be a model for supporting petascale simulation-based science and data-driven science."

When Stampede is deployed in 2013, it will be the most powerful system in the NSF XD environment, currently the most advanced, comprehensive, and robust collection of integrated digital resources and services enabling open science research in the world. As a critical part of XD, the Extreme Science and Engineering Discovery Environment (XSEDE) consortium comprising more than a dozen universities and two research laboratories, has now replaced the TeraGrid as the integrating fabric for the bulk of the NSF's high-end digital resources. Researchers from any U.S. open science institution can apply to use Stampede for a variety of novel scientific and educational activities through the XSEDE project.

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Staff

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Faith Singer-Villalobos
Public Relations
faith@tacc.utexas.edu

Watch a video of TACC Director Jay Boisseau discussing Stampede.
Stampede System Overview

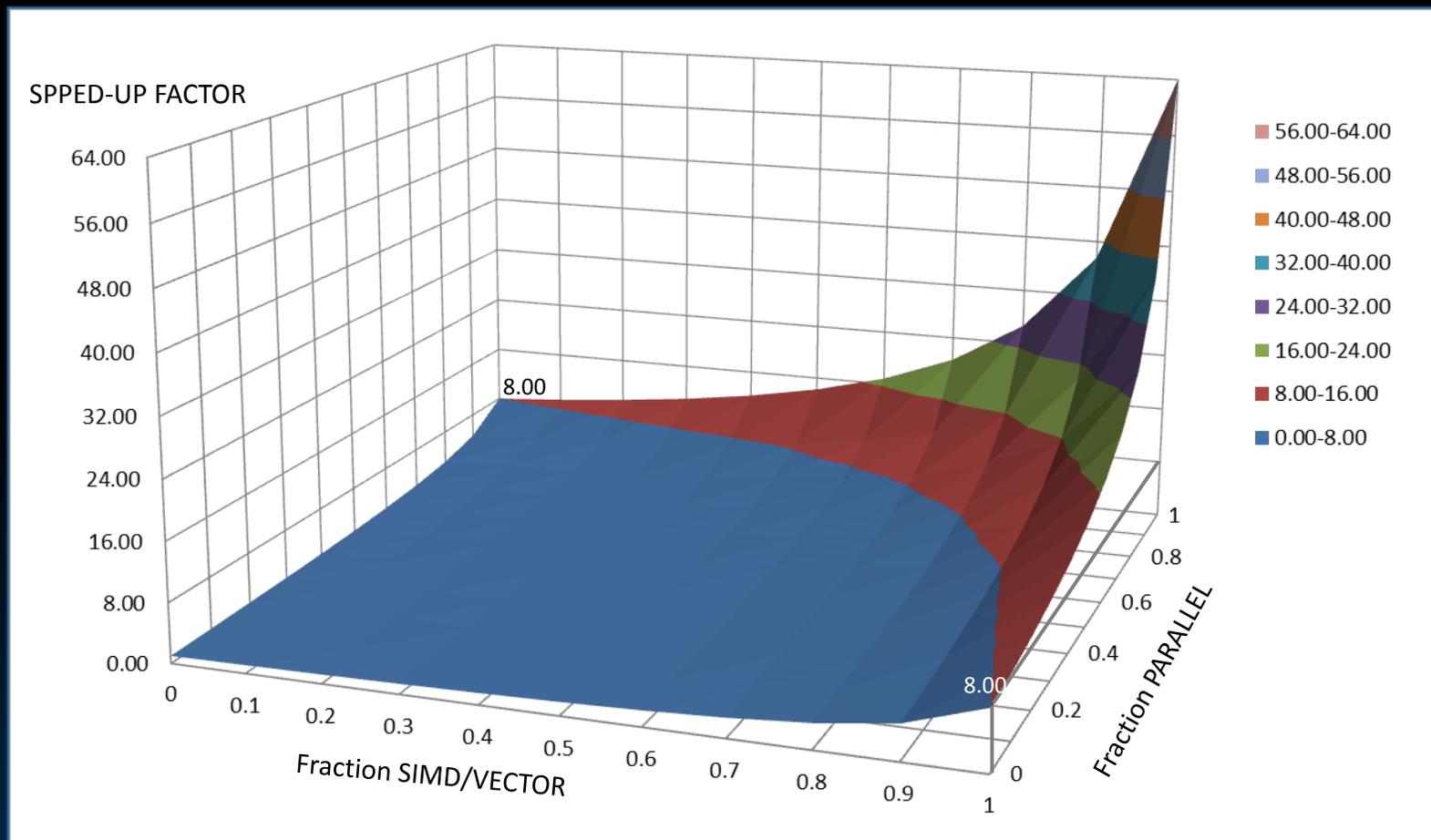
"Stampede"

(22.09.2011)

- 10 PFLOPS peak
- 272 TB memory
- 14 PB storage
- Deployment scheduled in 2013
- DELL* System
- Intel® Xeon® E5 (Sandy Bridge-EP) processors
- Intel® MIC (Knights Corner) co-processors
- FDR InfiniBand* (56Gb/s) cluster fabric

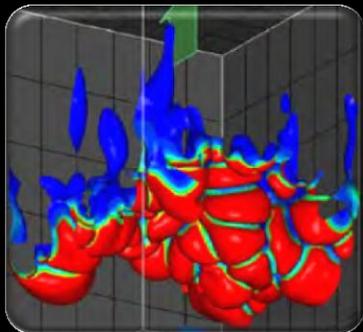
Example: Theoretical Speed-Up with 8 Cores and 8-way SIMD

Applying Amdahl's Law Twice



Assume Exascale Computing at 20MW ...

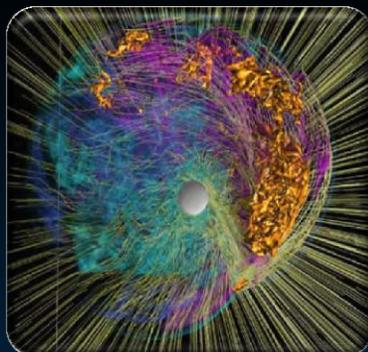
New Forms of Energy



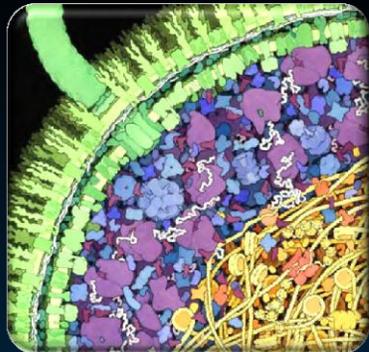
Ecological Sustainability



Space Exploration



Medical Innovation



And many others....

Data Center Sized Exascale System

Lower Volume
Higher Cost

20MW



Rack Sized Petascale System

“Mainstream”

20KW



Embedded Terascale System

Higher Volume
Lower Cost

20W

For illustration and concept only.



Intel's Plans For Exascale

Efficient Performance



Programming Parallelism



Extreme Scalability

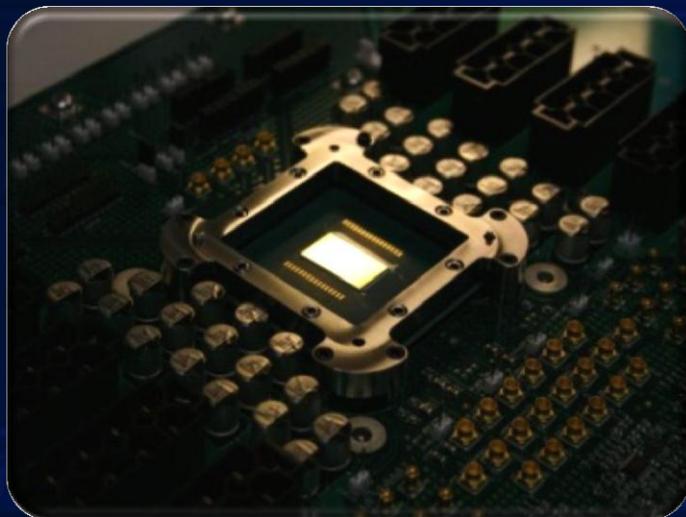


Intel Exascale Plans for 2018+:
>100X Performance of today at
only 2X the Power of today's #1 System
Scaling today's Software Models ...

All dates, data and figures are preliminary and are subject to change without any notice

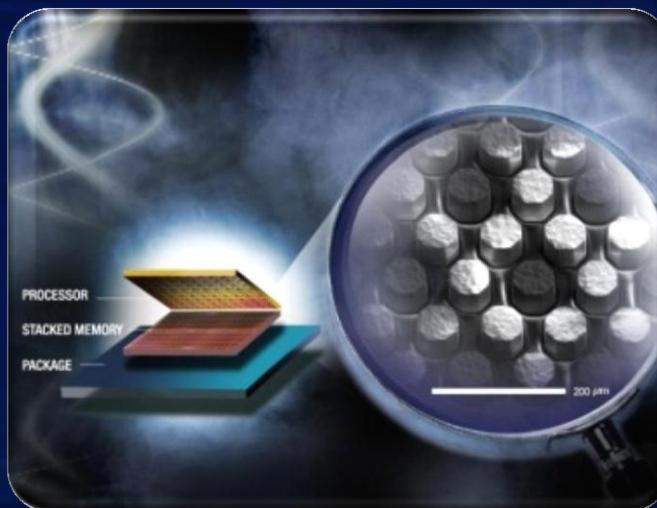
Intel TeraScale Research Areas

MANY-CORE COMPUTING



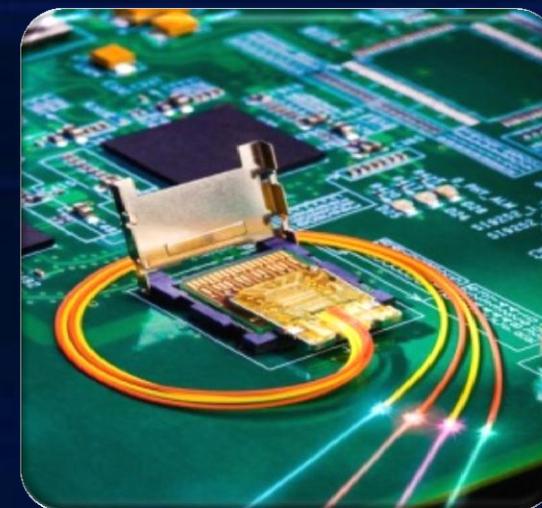
Teraflops
of computing power

3D STACKED MEMORY



Terabytes
of memory bandwidth

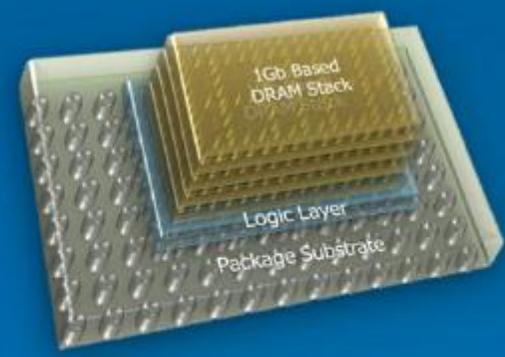
SILICON PHOTONICS



Terabits
of I/O throughput

For illustration only. Future vision, does not represent real products.

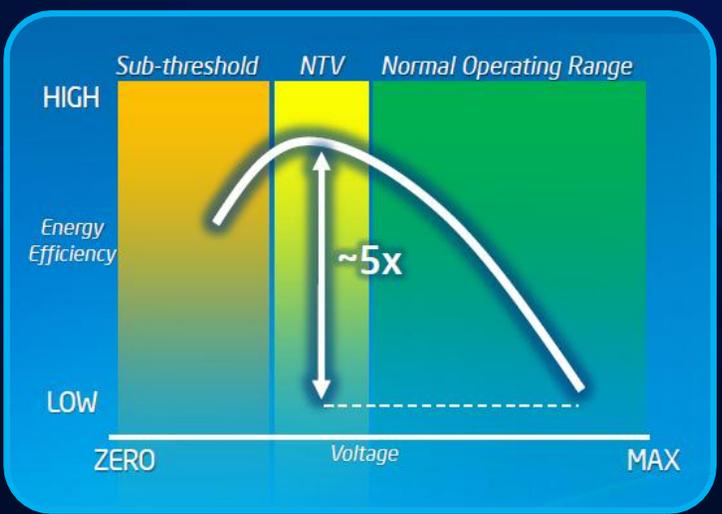
Near Threshold Voltage (NTV) Operation



Hybrid DRAM Stack



Micron
Research Collaboration
with Micron Technology



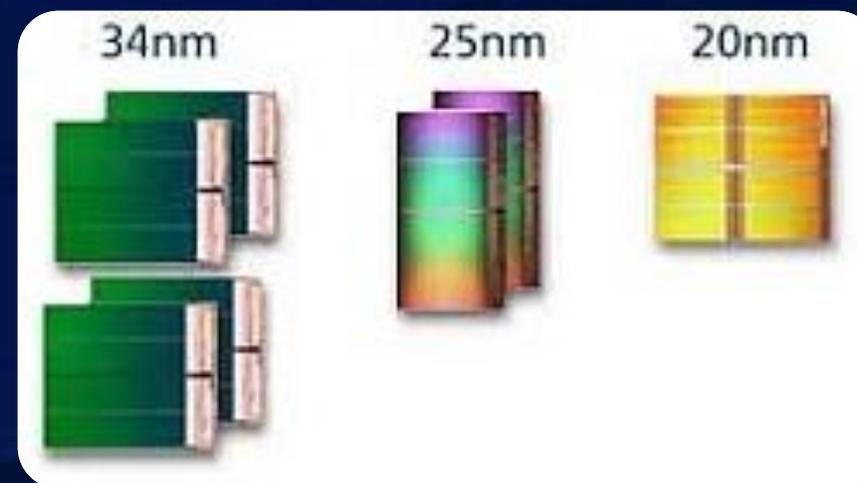
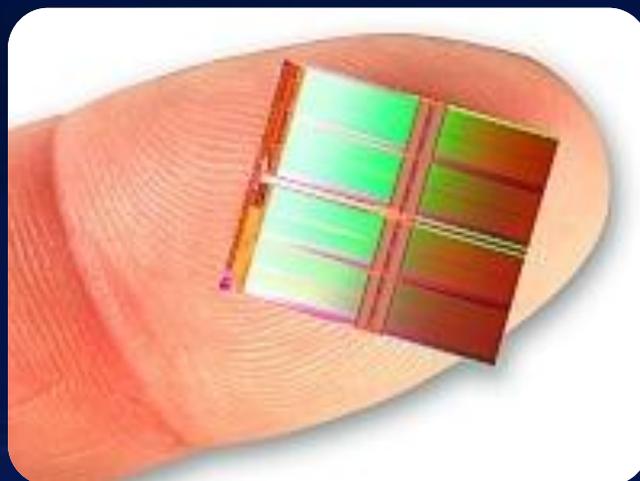
128GB/s (1Tb/s) Bandwidth 7x better energy efficiency than DDR3



Intel and Micron's Joint-Development Venture

IM Flash Technologies (IMFT)

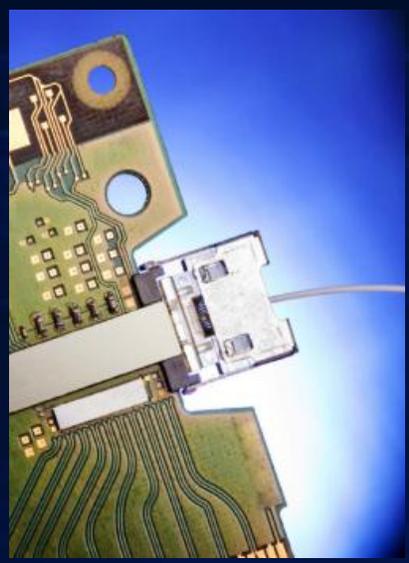
128 Gbit (16GB) NAND in 20nm



Pictures: Micron



Silicon Photonics



The Path to Tera-scale Data Rates

Today: 12.5 Gbps x 4 = 50Gbps

25 Gbps x 4 = 100Gbps

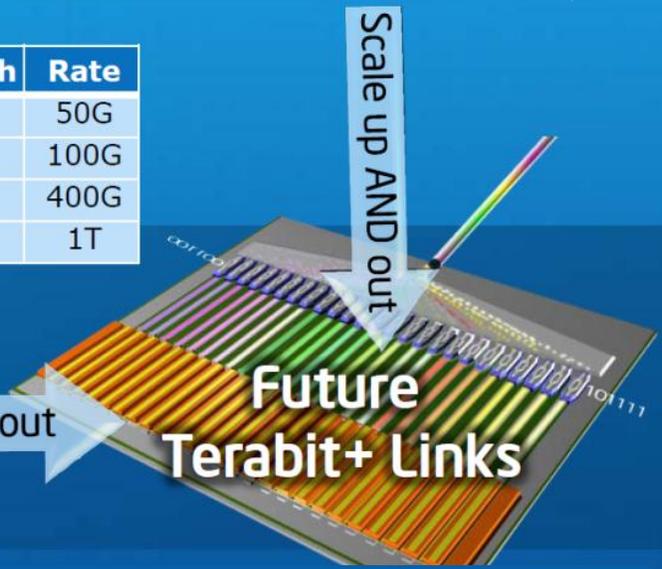


Speed	Width	Rate
12.5	x4	50G
12.5	x8	100G
25	x16	400G
40	x25	1T

12.5 Gbps x 8 = 100Gbps



x16, x32...



Scale up AND out

Future Terabit+ Links

Could enable cost-effective high speed I/O for data-intensive applications



Thank You.

