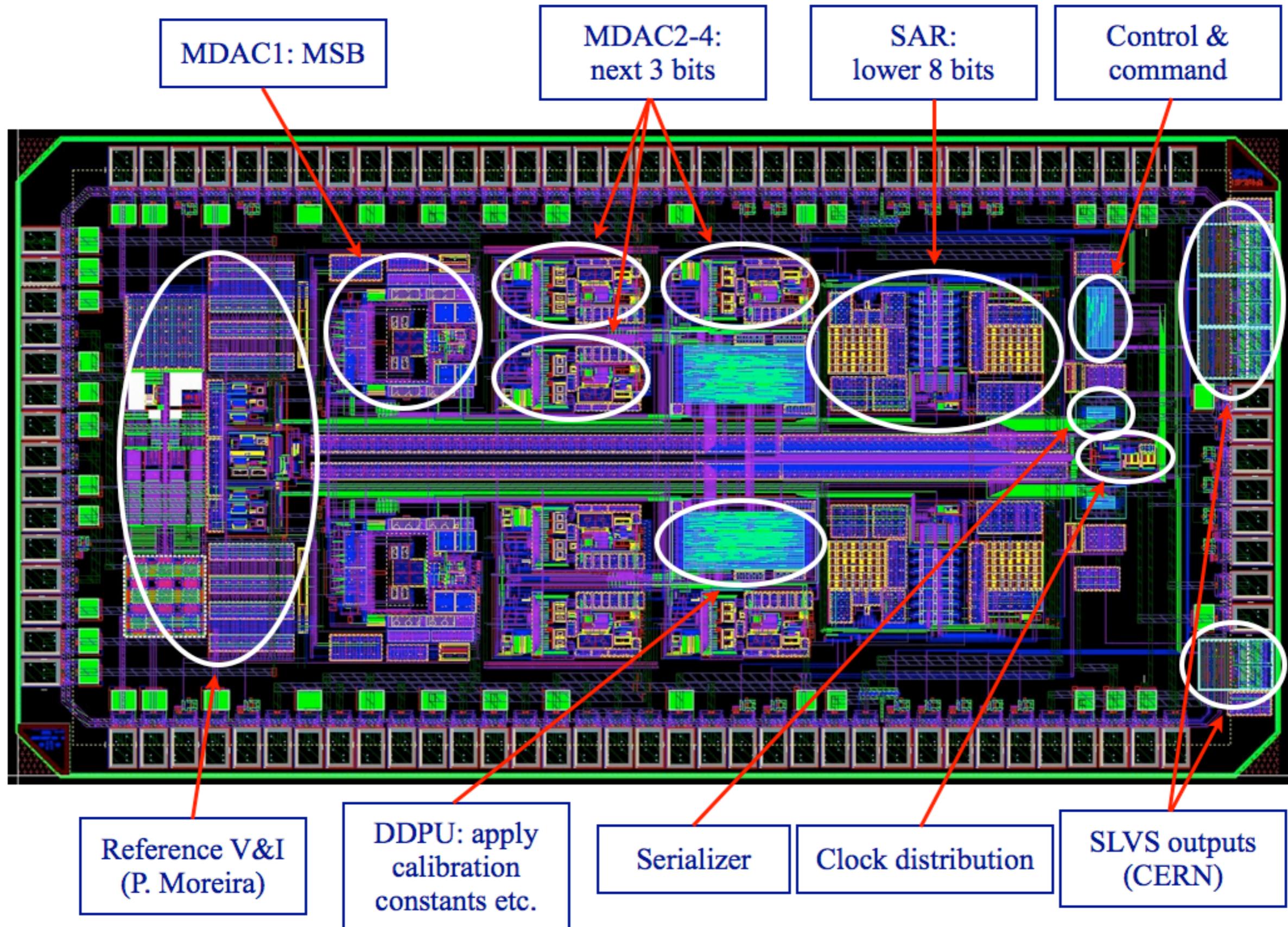


FY13 Nevis R&D Budget: Tasks

- ADC development:
 - Submission of nevis12 chip on Nov 5th
 - Reduced to two channels because of I/O frame size: need many many test outputs that will not exist on production chip
 - Design & fabrication of test boards → April 1
 - Nevis12 testing → December (?) mainly by physicists
 - NevisADC prototype design: April 2013 → August 2014
- Clock & slow control fanout chip
 - Design, layout and submission of prototype: November 2012 → August 2013

Nevis12 Chip

3.7 x 1.9 mm²



WBS

WBS	description	milestone	start date	stop date	FTE (name)	other src (name)
1133	ADC			10/15/16		
1133.1	Nevis12 chip			12/31/13		
1133.1.1	design	submission	10/1/12	11/5/12	2 (EE, Ban, Sippach), 1 (ES, Kuppambatti)	
1133.1.2	precision testboard	fabricated and tested	11/5/12	4/1/13	(EE, Ban, Sippach), (ES, Kuppambatti, ET, Bishop)	0.5 (Phy, Andeen, Thompson)
1133.1.3	functionality testboard	fabricated and tested	11/5/12	4/1/13	(EE, Ban, Sippach), (ET, Bishop)	0.1 (Phy, Andeen, Thompson)
1133.1.4	chip functionality tests	chips selected	4/1/13	4/5/13	(EE, Ban, Sippach), (ES, Kuppambatti, ET, Bishop)	0.5 (Phy, Andeen, Thompson)
1133.1.5	final assembly	chips on precision board	4/5/13	4/15/13	(EE, Ban, Sippach), (ES, Kuppambatti, ET, Bishop)	
1133.1.6	chip testing	fully characterized	4/15/13	12/31/13	(EE, Ban, Sippach), (ES, Kuppambatti, ET, Bishop)	1.0 (Phy, Andeen, Thompson, student)
1133.2	NevisADC prototype		4/15/13	9/1/15		
1133.2.1	design	submission	4/15/13	8/15/14	(EE, Ban, Sippach), (ES, Kuppambatti)	
1133.2.2	precision testboard	fabricated and tested				
1133.2.3	functionality testboard	fabricated and tested				
1133.2.4	chip functionality tests	chips categorized				
1133.2.5	final assembly	chips on precision board				
1133.2.6	chip testing			9/1/15		
1133.3	NevisADC production					
1133.3.1	PRR	PRR	9/15/15	9/15/15		
1133.3.2	production	production complete	10/1/15	10/1/16		
1133.3.3	QC & chip categorization	QC complete	1/1/16	10/15/16		
11361	FE Clock Fanout		11/5/12			
11361.1	test chip					
11361.1.1	design	submission	11/5/12	8/15/13	(EE, Ban, Sippach), (ES, Kuppambatti)	

Costs

- Labor: 2 FTE EE, 1 FTE E student, 0.5 FTE ET, 0.17 FTE Instrumentation physicist (help set up teststands)
 - US\$ 519,589
- Other costs: M&S \$80k + travel \$9,440

M&S	Item	cost	Travel	#.trips. domestic	d. travel cost	#.trips.foreign	f. travel cost
FY13	Nevis12	30000	FY13	2	2240	3	7200
	Clock FO testchip	10000	FY14	2	2240	3	7200
	testboards	20000	FY15	2	2240	3	7200
	test equipment	20000	FY16	2	2240	3	7200
			FY17	2	2240	3	7200
			FY18	2	2240	3	7200
			total		13440		43200

Save?

- Can move clock FO submission to FY14:
 - Save ~\$15k M&S + some labor since slow down design work, \$30-\$50k depending how many EE months we move to FY14
- Not much room in ADC schedule if want to meet late 2015 PRR date